March 30, 2003, Sunday Tutorials

Location:	Room: Landmark A	Room: Landmark B	Room: Landmark C
8:00–9:30 a.m.	111: An Introduction to Semiconductor Reliability—Vijay Reddy, TI	121: ESD Basics—Charvaka Duvvury, TI	
10:00–11:30 a.m.		122: ESD Testing and Failure Analysis for Semiconductor IC's— Jonathan Brodsky, TI	
Lunch Break			
1:30–3:00 p.m.	112: Introduction to Predictive WLR—Eric Snyder, Sandia Technologies	123: ESD High Current Phenomena, Modeling and Process Effects— Gianluca Boselli, TI	131: Problems & Solutions for FA on Advanced Microelectronic Circuits—Chris Henderson, Sandia Nat'l Labs
3:30–5:00 p.m.		124: Advanced ESD Protection Design— Charvaka Duvvury, TI	132: Optical Tools for IC Failure Analysis — Ed Cole, Jr., Sandia Nat'l Labs

March 31, 2003, Monday Tutorials

Location:	Room: Landmark A	Room: Landmark B	Room: Landmark C	Room: Landmark D
8:00–9:30 a.m.	211: Reliable Plastic Encapsulated Microcircuits for Harsh Environments—Chuck Reusnow Lockheed Martin Missiles & Fire Control and Brian Russell, Dow Corning	221: Dielectric Rel Models & Mechanisms — Paul Nicollian TI	231: Integration Challenges of Cu Low k Integration — Glenn Alers, Novellus	
10:00–11:30 a.m.		222: Physics of soft-breakdown and implications for ICs Ashraf Alam, Bell Labs	232: Current Challenges of Cu Electromigration Reliability—Christine S. Hau-Riege, AMD	241: NBTI challenges in PMOSFETs of Advanced CMOS Technologies—Guiseppe La Rosa, IBM Microelectronics
Lunch Break				
1:30–3:00 p.m.	212: Reinventing CMOS: Physics, Reliability and The Roadmap— Ted Dellin, SNL	223: Ultra thin oxide reliability in CMOS devices & circuits—Jim Stathis, IBM	233: Impact of Low k on EM Reliability for Cu Interconnects— Paul Ho, U.T. Austin	242: SER Program—Daniel Chesire 1. Robert Baumann, TI 2. Steve Wender, Los Alamos 3. Fred Sexton & Paul Dodd, Sandia 4. Mike Tucker, Alpha Sciences 5. Charles Slayman, Sun Microsyst.
3:30–5:00 p.m.		224: Issues in high k rel—Robin Degraeve, IMEC	234: Interfacial Adhesion and its Impact on Cu Interconnect Reliability—Michael Lane, IBM	