



Eliminating the Threat of Soft Errors – A System Vendor Perspective

**IRPS SER Panel Discussion
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OUTLINE

- Urgency of the problem
- Roles and responsibilities
- System manufacturer's demands
- Semiconductor industry compliance
- Information sharing
- Conclusions

IMPORTANCE/URGENCY

- Server customers are demanding higher reliability and better performance (read more memory but fewer fails)
- The semiconductor industry as a whole is only beginning to understand cosmic ray upset
- Sun can take steps to mitigate cosmic ray upset only if our component vendors can forecast what the failure mechanisms are

ROLES/RESPONSIBILITIES

- Merchant Semiconductor (Typical DRAM, some SRAM)

- * Develop good design and process rules to minimize SER
- * Gear up to do routine accelerated beam measurements (or contract with third party test houses) on product

- Fabless Design / IP / Silicon Foundry (some SRAM)

- * Develop cooperative process to mimic what merchant commodity vendors will do (ie good SER designs/libraries, SER characterization of silicon process, develop confidence in modeling)

- Systems Design (ie Sun Microsystems)

- * Communicate clearly what SER events we can design around, what events we can detect but not correct and what events will go undetected – errors in datapaths vs more serious errors in command/address paths (silent data corruption)
- * Make sure SER events are really due to memory and not other components in data path
- * Specifying one FIT number **WILL NOT WORK**. It's too simplistic!

- University/R&D

- * Better understanding/characterization of energy spectra and flux of high energy and thermal neutrons

SYSTEM MANUFACTURER DEMANDS

- Fault tolerant server designs only work if the right fault mechanisms have been accounted for
- Single bit soft errors from alpha particles or cosmic rays are an excellent example – single error correct/double error detect (SEC/DED) code is implemented on commodity DRAM with only ~10% overhead.
- What other upset mechanisms are going to occur? Will they be "fatal"? (ie Silent data corruption? System crash?)
- What is the FIT of "fatal" upsets? Less than hard fail FIT?
- How will these "fatal" soft errors scale with sub-0.1um designs?

Compliance/Qualification/Best Practices

- **JEDEC Standard** JESD89 "Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices" (<http://www.jedec.org/download/default.cfm>) – multi-energy neutron beam measurements are critical
- **JEITA** working on a document to be published this year
- **Foundries** develop measurement and models to go along with design library
- **Design Houses/IP** to develop tools to simulate SER upset (neutron beam measurements might not be practical for small volume parts)
- **Large volume commodity** parts like DRAM and SRAM, neutron beam measurements should become standard. But what to measure? Cell upset is interesting, but not critical with SEC/DED protection.

Information Sharing

- Reducing SER below what systems designs require to meet RAS targets offers no competitive advantage (ie Sun will not pay more for a 1 FIT DRAM vs 10 FIT DRAM if our design is capable of handling 30 FIT)
- It's more important that vendors and users agree on the SER characterization techniques, how to interpret them and where this is leading us..... than it is to get a low FIT score
- Industry consensus of measurement and models is more important than getting a low FIT score
- Therefore, sharing information, building an understanding of measurement techniques, device physics models and forecasting performance becomes paramount

CONCLUSIONS

URGENCY - Cosmic ray upset is real and observable in large memory systems.

ROLES/RESPONSIBILITIES – Everybody from the fabless designer to the system designer own a piece of the puzzle.

SYSTEM DESIGN DEMANDS - For large memory with SEC/DED, cell upset FIT is a "don't care." What's important is the next layer of SER FITs buried beneath this. What mitigating steps can be taken in the system design to eliminate this threat?

COMPLIANCE - Build on JEDEC and JEITA methods.

INFORMATION SHARING - Consensus of techniques and interpretation is more important than claiming the lowest FIT!