



IRPS 2003

# HANDLING DRAM AMNESIA

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# Actions During Development

(Before first silicon)

- Substrate engineering  
(gathering efficiency for charge)
- Wafer process development  
(high storage capacitance)
- Circuit + design development  
(critical charge of nodes)
- Cell concept optimized
- Simulation of critical charge of nodes

# Component Tests

(After first silicon)

- SSER: only slow systems available for soft error tests  
extrapolation. to w.c. cond. → loss in accuracy
- ASER: appropriate alpha source is necessary  
possible degradation from TDD
- PSER: problems with low-energy particles  
suitable for relative tests
- NSER: best practice (LANL) —  
but a fast mobile tester is needed with  
a DUT socket separated from the electronics

# Comparison of Test Results

(256M SDRAM)

**ASER** < 0.04 FIT  
**NSER** < 10.2 FIT

> together: SER < **11FIT** (w.c.)

**SSER** < 65 FIT(60% C.L.)= < 500 FIT(75ns;N.Y.)  
(more than 14 million device hours!)  
< **1600 FIT** (N.Y.; 95% C.L.) JESD89

System soft error tests are not useful for DRAMs  
Soft errors from Cosmic Radiation are dominant  
95% C.L. is unbearable for DRAMs

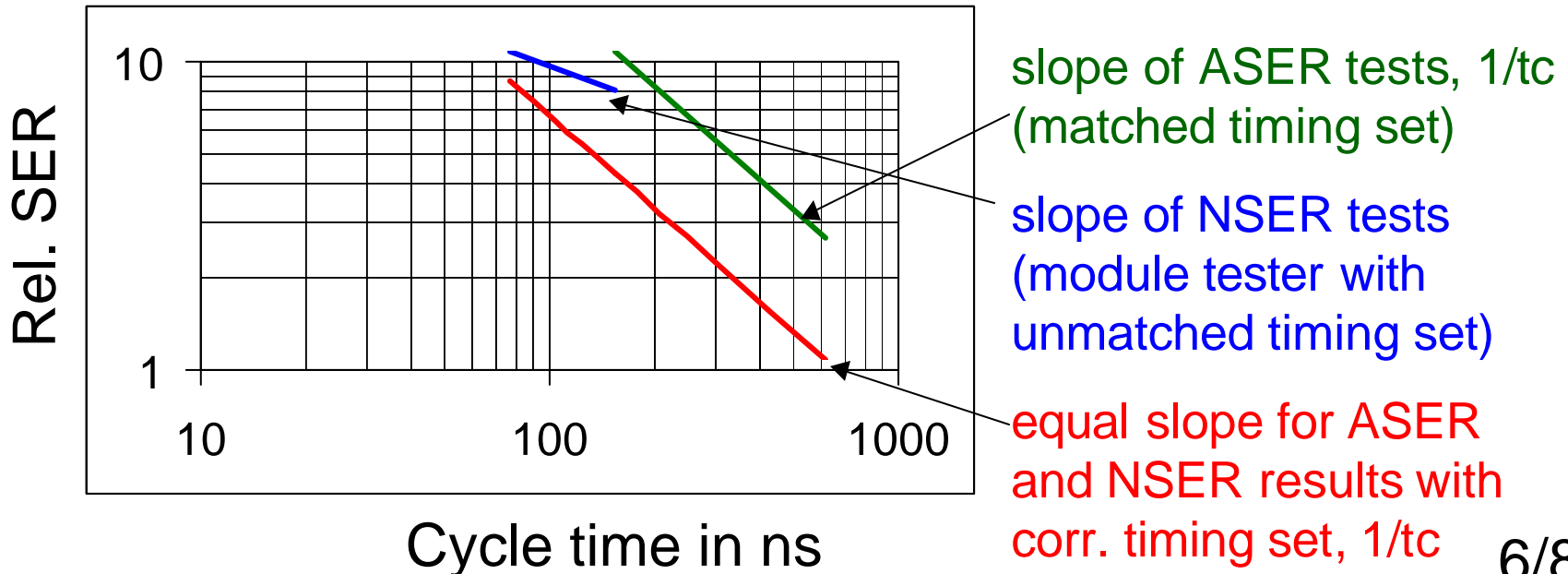
# Multi-bit Soft Errors in DRAMs

(Neutron Beam Tests with Samples from 4 Vendors)

	<b>Soft Errors from Cell Array Hits</b>	<b>Soft Errors from Hits in Peripheral Circuits</b>
<b>Error Signature</b>	<b>single-bit, double-bit, bit-cluster</b>	<b>word line, bit line</b>
<b>Erase Error</b>	<b>re-write</b>	<b>power down + up, write</b>
<b>Fail-bit per Event</b>	<b>majority = 1bit (up to 16 bit)</b>	<b>several K-bit (2K-bit to 8K-bit)</b>
<b>Cycle Dependence of Error Rate</b>	<b>depends on cell weakness (from indep.of cycle time to proport. to 1/cycle time)</b>	<b>depends on hit node (e.g. 1/cycle time)</b>
<b>Error Rate</b>	<b>4 FIT to 800 FIT (N.Y., 60% C.L.)</b>	<b>&lt; 0.2 FIT to 2 FIT (N.Y., 60% C.L.)</b>

# Suitable Test Program

For cycle dependence of DRAMs the cycle of sense amp. activations is important not the clock cycle. All cycle times (read, refresh, change of address, etc.) have to be equal for a clear dependence between test frequency and SER.



# Information Sharing

## Component side

- Error rate
- Number of failbit per error
- Distribution of failbit per error

## System Side

- What is tolerable (frequency for each distribution of failbit)
- Costs of widening the limit of tolerance

Cost-effective reduction of the SER

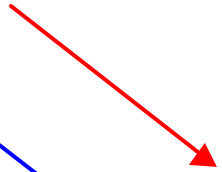
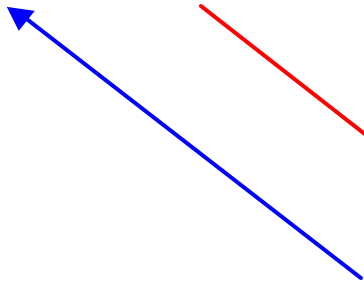
# Conclusion

## Component Side

Optimize rate and  
signature of errors

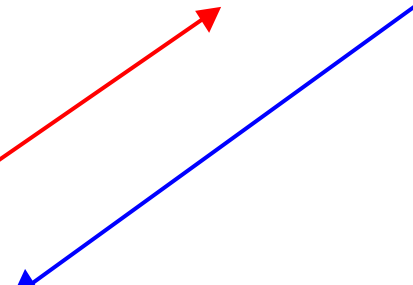
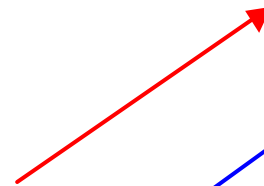
## System Side

Optimize  
error tolerance



for systems

for components



Each side has to take the features of the other side into account