

Monday 2004 Tutorial Program

	Future CMOS	Gate Dielectrics	Low K/Cu Intercon.	RF/MMIC Rel.	Failure Analysis
AM1	201. Trends and Challenges in Device Scaling and Circuit Design D. Cox, IBM	211. Oxide BD Methods and Models R. Vollertsen Infineon	221. Low K/Cu Integration G. Dixit Applied Materials	231. Microwave/RF MMIC Rel. Physics and Test Methods J. Scarpulla Aerospace Corp.	241. Failure Analysis: Current Processes and Future Needs L. Wagner TI
AM2	202. Future Direction & Challenges for Flash Memory Scaling G. Atwood/S. Lai Intel	212. Oxide BD in CMOS Devices and Circuits J. Stathis IBM	222. Cu Interconnect Processing Challenges W.Y. Hsu Applied Materials	232. MMIC Manufact. and Packaging Rel. Issues W. Roesch TriQuint	242. Failure Site Isolation Methods D. Vallett, IBM & E. Cole, Sandia
PM1	203. Reinventing CMOS T. Dellin Sandia National Laboratory	213. Multiple-BD Statistics & Post-BD Rel. Methodology J. Suñé, U. Auto. Barcelona	223. Electromigration Reliability P. Ho U.T.	233. SiGe and Si RF CMOS Reliability W. Abadeer IBM	
PM2		214. Rel. Issues on High-K Diel. – What is Different from SiO ₂ H. Satake Toshiba	224. Via Stress Migration G. Alers Novelus	234. HBT Reliability: Comparison of SiGe, GaAs, and InP Technology F. Guarin IBM	