2008 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

April 27 - May1, 2008 • Phoenix Civic Plaza Convention Center / Hyatt Regency Phoenix at Civic Plaza • Phoenix, Arizona

CALL FOR PAPERS and CALL FOR POSTERS

IRPS offers its attendees technical sessions, tutorials, workshops, a year-in-review seminar and a poster session, all covering state-of-the-art developments in electronic and optoelectronic reliability**. Attendees returning from IRPS will be better equipped to solve critical reliability problems and develop effective qualification procedures that affect their companies' bottom line.**

YOUR ORIGINAL PAPERS AND POSTERS ARE SOLICITED, which:

A. Identify new or improve our understanding and modeling of failure mechanisms in electronic and optoelectronic devices, materials, and systems;
B. Identify how fabrication processes influence the susceptibility of the product to particular failure mechanisms;
C. Quantify the impact of device and circuit design, as well as material and process selection on reliability;
D. Present new, innovative, or improved failure analysis techniques. Provide new modeling and simulation of failure mechanisms;
E. Describe reliability testing/stressing, qualification, and screening methodologies or strategies for materials, devices, circuits, or chips; either at wafer- or module-level for "commercial" or "extreme" environments;
F. Demonstrate techniques to build-in or extend reliability while meeting performance goals, especially as technologies are scaled.

For Silicon (Integrated Circuits, Discrete Devices, MEMS), Non-Silicon (GaAs, LEDs and Diode Lasers, Optical Fiber and Flat Panel Displays), and Emerging Technologies Including Organic Electronics and Nanotechnology IN THE FOLLOWING AREAS:

PRODUCT

Product Reliability and Burn-in – Product (Chip-level) Reliability Issues; New or Novel Failure Modes in Logic/ Memory ICs, Burn-In Elimination Strategies, Wafer-Level Burn-In; Correlation Between Yield, Infant Mortality, Burn-In Fallout, Technology Model Predictions

Non-Volatile Memory – Unique Reliability Phenomena and Failure Mechanisms in Non-Volatile Memories; Reliability of Ferroelectric or Magnetic Memory Cells or Arrays

Qualification Strategies – New Techniques, Test Structures, and Product Vehicles for Technology or Chip Qualification; Best Practices to Reduce Cost and/or Time-to-Market; "Commercial" or "Extreme" Environments

Circuits – Comprehending Reliability in Designs and Circuits; Soft Error Upsets; Analog Circuit Reliability Issues; Simulation/Modeling Techniques

Assembly and Packaging – Package/Assembly Reliability, Stress Modeling, Cu and Low-k Issues, Chip Scale Integration, BGA and Flip Chip Assembly; Bump Reliability Issues

Failure Analysis – Evidence of New Failure Mechanisms and Failure Analysis Techniques, Case Histories

MEMS – Reliability of New Structures, Sensors, Actuators; Reliability Testing and Analysis of MEMS Systems; Design and Processing for Reliability

PROCESS

Device and Process - Reliability Driven Process Interactions; New Process-Related Reliability Issues. Including Si, and Non-Si based, OptoElectronics; MEMS, High Voltage devices and Nanotechnology

Transistor – New Hot Carrier Phenomena; NBTI; Transistor Scaling Issues; Impact of Alternative Gate Dielectrics; Effect of Materials' Degradation; Silicon on Insulator (SOI) Reliability Issues; High Performance Transistor Reliability; Mobility Enhancement Techniques such as Strained Si; Metal Gate Integration and TFT Devices

Interconnects – Defect and Wearout Phenomena in Cu and Al Systems; Low-k/Oxide Inter/Intra-Level Reliability; Mechanical Stress Related Reliability Issues; Joule Heating Effects; Modeling Mechanical & Thermal Behavior; Fast/Slow Stress Correlations

Device Dielectrics – Oxide Breakdown Mechanisms;New or Novel Dielectric Materials Reliability; Processing Interactions; Wearout Models; Gate Dielectric Thickness Scaling; Stress Methodologies; Multiple Dielectric Technologies

ESD and Latch-Up – Novel Structures including SOI and Bipolar; Damage Interpretation; Circuit/Process Improvements; Scaling Issues, RF CMOS

Process Induced Damage – Reliability Degradation Associated with Damage; Early Non-Destructive In-Line Detection and Reliability Analysis

Nanoelectronic Device Reliability – Drift & wear-out phenomenon associated with novel and future device structures including FINFET, carbon nanotube FET, semiconductor wire FET, molecular devices, and hybrid technologies.

PAPER AND POSTER SUBMISSION INSTRUCTIONS

Abstracts Must Be Received By: October 5, 2007

Abstract/Paper/Poster Submission: Your submission of original work should clearly and concisely state the specific results, why they are important, and how they relate to prior work. An on-line IRPS document template, located at http://www.tpc.irps.org is available and will save you time.

For papers: Only two-page abstracts will be accepted. Abstract submissions should include enough information to clearly indicate the path to develop a final paper.

For posters: you may submit up to two pages. If accepted, poster submissions will be included in the symposium proceedings as a two-page narrative. The technical committees reserve the right to accept paper submissions as posters.

For all submissions: complete a cover page that includes the following: a 50 word summary of your work, the technical category of submission; the type of submission (paper or poster); affiliations of all authors and contact information. A template for this cover page is located at http://www.tpc.irps.org.

Late Paper Submission: A limited number of late breaking news full-length manuscripts will be considered on a space available basis. Completed manuscripts may be submitted until December 7, 2007. These manuscripts are to follow the criteria for accepted papers above. Accepted late papers will be included in the conference proceedings and in the technical presentations at the conference.

Electronic Submission Procedures: Please follow electronic instructions on the IRPS Web page http://www.tpc.irps.org. Send electronic submissions to technical.chair@irps.org. All submissions will be acknowledged by e-mail within two weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair. If it is not possible to send your submission electronically, please contact the Technical Program Chair to make other arrangements.

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