2009 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

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CALL FOR PAPERS and CALL FOR POSTERS

IRPS offers its attendees technical sessions, tutorials, workshops, a year-in-review seminar and a poster session, all covering state-of-the-art developments in the reliability physics of electronic and optoelectronic devices, materials, and systems. **Attendees returning from the IRPS will be better equipped to solve critical reliability problems and develop effective qualification procedures that affect their companies' bottom line.**

YOUR ORIGINAL PAPERS AND POSTERS ARE SOLICITED, which:

A. Identify new or improve our understanding of the physics of failure and modeling of mechanisms in electronic and optoelectronic devices, materials, and systems;
B. Identify how fabrication processes influence the susceptibility of product to particular physical failure mechanisms;
C. Quantify the impact of device and circuit design, as well as material and process selection on reliability;
D. Present new, innovative, or improved failure analysis techniques;
E. Describe reliability testing/stressing, qualification, and screening methodologies or strategies for materials, devices, circuits, or chips; either at wafer- or module-level for commercial or "extreme" environments;
F. Demonstrate techniques to build-in or extend reliability while meeting performance goals, especially as technologies are scaled.

For Silicon (Integrated Circuits, Discrete Devices, MEMS, TFTs), Compound Semiconductor (Bipolar, BiCMOS, LEDs and Diode Lasers), and emerging technologies including Organic Electronics and Nanotechnology IN THE FOLLOWING AREAS:

PRODUCT

Product Reliability and Burn-in – Product (Chip-level) Reliability Issues; New or Novel Failure Modes in Logic/ Memory ICs, Burn-In Elimination Strategies, Wafer-Level Burn-In; Correlation Between Yield, Infant Mortality, Burn-In Fallout, Technology Model Predictions

Non-Volatile Memory – Unique Reliability Phenomena and Failure Mechanisms in Non-Volatile Memories; Reliability of Ferroelectric, Magnetic, Phase Change, and Charge Trapping Memory Cells or Arrays

Qualification Strategies – New Techniques, Test Structures, and Product Vehicles for Technology or Chip Qualification; Best Practices to Reduce Cost and/or Time-to-Market; "Extreme" Environments (Temperature, Radiation, Humidity, etc.); Best Practices for Fabless Semiconductor Companies

Circuits – Comprehending Reliability in Designs and Circuits; Physics of Soft Error Upsets; Analog Circuit Reliability Issues; Simulation/Modeling Techniques

Assembly and Packaging – Package/Assembly Reliability, Stress Modeling, Cu and Low-k Issues, Chip Scale Integration, BGA and Flip Chip Assembly; Bump Reliability Issues

Failure Analysis – Evidence of New Failure Mechanisms; Failure Analysis Techniques; Case Histories

MEMS – Reliability of New Structures, Sensors, Actuators; Reliability Testing and Analysis of MEMS Systems; Design and Processing for Reliability

PROCESS

Device and Process - Reliability Driven Process Interactions; New Process-Related Reliability Issues and Associated Physics of Failure. Including Si, and NonSi based, OptoElectronics; MEMS, High Voltage devices and Nanotechnology

Transistor – New Hot Carrier Phenomena; NBTI and PBTI; Transistor Scaling Issues; Impact of Alternative Gate Dielectrics; Effect of Materials' Degradation; Silicon on Insulator (SOI) Reliability Issues; High Performance Transistor Reliability; Mobility Enhancement Techniques such as Strained Si; Metal Gate Integration and TFT Devices

Interconnects – Defect and Wearout Phenomena in Cu and Al Systems; Low-k/Oxide Inter/Intra-Level Reliability; Mechanical Stress Related Reliability Issues; Joule Heating Effects; Modeling Mechanical & Thermal Behavior; Fast/Slow Stress Correlations

Device Dielectrics –Breakdown Mechanisms; New or Novel Dielectric Materials Reliability; Processing Interactions; Wearout Models; Gate Dielectric Thickness Scaling; Stress Methodologies; Multiple Dielectric Technologies

ESD and Latch-Up – Novel Structures including SOI and Bipolar; Damage Interpretation; Circuit/Process Improvements; Scaling Issues, RF CMOS

Process Induced Damage – Reliability Degradation Associated with Damage; Early Non-Destructive In-Line Detection and Reliability Analysis

Nanoelectronic Device Reliability – Drift & wear-out phenomenon associated with novel and future device structures including FINFET, carbon nanotube FET, semiconductor wire FET, molecular devices, and hybrid technologies.