



2004 INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM

April 25-30, 2004 • Hyatt Regency Phoenix at Civic Plaza • Phoenix, Arizona

CALL FOR PAPERS and CALL FOR POSTERS

IRPS offers its attendees high quality technical sessions, tutorials, workshops, a poster session, and a half-day "Reliability-Year-In-Review" seminar, all covering state-of-the-art developments in electronic and optoelectronic reliability. **Attendees returning from IRPS will have enhanced knowledge in uncovering and solving state of the art reliability issues affecting present day products as well as directing future design methodologies.**

YOUR ORIGINAL PAPERS AND POSTERS ARE SOLICITED, which:

- A. Identify new, or improve our understanding and modeling of, mechanisms of failure in electronic and optoelectronic devices and materials;
- B. Identify how fabrication processes influence the susceptibility of the product to particular failure mechanisms;
- C. Quantify the impact of device and circuit design, as well as, material, and process selection on reliability;
- D. Present new, innovative, or improved failure analysis techniques. Provide new theoretical modeling and simulation of failure mechanisms;
- E. Describe reliability testing/stressing, qualification, and screening methodologies or strategies for materials, devices, circuits, or chips; Either at wafer- or at module-level;
- F. Demonstrate techniques to build-in or extend reliability while meeting performance goals, especially as technologies are scaled.

For Silicon (Integrated Circuits, Discrete Devices, MEMS) and Non-Silicon (GaAs, LEDs and Diode Lasers, Optical Fiber and Flat Panel Displays) Devices IN THE FOLLOWING AREAS:

PRODUCT

Product Reliability and Burn-in – Product (Chip-level) Reliability Issues; New or Novel Failure Modes in Logic/Memory ICs, Burn-In Elimination Strategies, Wafer-Level Burn-In; Correlation between Yield, Infant Mortality, Burn-In Fallout, Technology Model Predictions

Non-Volatile Memory – Unique Reliability Phenomena and Failure Mechanisms in Non-Volatile Memories; Reliability of Ferroelectric or Magnetic Memory Cells or Arrays

Qualification Strategies – New Techniques and test structure and product vehicles for Technology or Chip Qualification; Best Practices to Reduce Cost and/or Time-to-Market

Circuits – Comprehending Reliability in Designs and Circuits; Soft Error Upsets; Analog Circuit Reliability Issues; Simulation/Modeling Techniques

Assembly and Packaging – Package/Assembly Reliability, Stress Modeling, Cu and Low-K Issues, Chip Scale Integration, BGA and Flip Chip Assembly; Bump Reliability Issues

Failure Analysis – Evidence of New Failure Mechanisms and Failure Analysis Techniques, Case Histories

MEMS – Reliability of New Structures, Sensors, Actuators; Reliability Testing and Analysis of MEMS Systems; Design and Processing for Reliability

PROCESS

Device and Process - Reliability Driven Process Interactions; New Process-Related Reliability Issues. Including Si, and Non Si based, OptoElectronics; MEMS

Transistor – New Hot Carrier Phenomena; NBTI; Transistor Scaling Issues; Impact of Alternative Gate Dielectrics; Effect of Materials Degradation Mechanisms; Silicon on Insulator (SOI) Reliability Issues; High Performance Transistor Reliability; Mobility enhancement techniques such as Strained Si. Metal gate integration and TFT devices

Interconnects – Defect and Wearout Phenomena in Cu and Al Systems; Low-k/Oxide Inter/Intra-Level Reliability; Mechanical Stress Related Reliability Issues; Joule Heating Effects; Modeling Mechanical & Thermal Behavior; Fast/Slow Stress Correlations

Device Dielectrics – Oxide Breakdown Mechanisms; New or Novel Dielectric Systems Reliability; Processing Interactions; Wearout Models; Gate Dielectric Thickness Scaling; Stress Methodologies; Multiple dielectric products.

ESD and Latch-Up – Novel Structures including SOI and Bipolar; Damage Interpretation; Circuit/Process Improvements; Scaling Issues, RF CMOS

Process Induced Damage – Reliability Degradation Associated with Damage; Early non-destructive In-Line Detection and Reliability Analysis

PAPER AND POSTER SUBMISSION INSTRUCTIONS

Abstracts Must Be Received By: October 24, 2003

Abstract/Paper/Poster Submission: Your submission of original work should clearly and concisely state the specific results, why they are important, and how they relate to prior work. An on-line IRPS [document template](http://www.irps.org/tpc), located at <http://www.irps.org/tpc> is available and will save you time.

For papers: submit a two-page abstract or a final manuscript of unrestricted length. Abstract submissions should include enough information to clearly indicate the path to develop a final paper.

For posters: you may submit up to two pages. If accepted, posters will be included in the proceedings as a two-page narrative. Posters will be presented during the Tuesday evening reception. Posters provide an opportunity for work in progress to be discussed at the symposium. Posters are also an ideal format for students to present the results of their research. The technical committees reserve the right to accept paper submissions as posters, in which case you may be asked to revise your manuscript such that it conforms to the two-page poster requirements.

For all submissions: complete a cover page that includes the following: a 50-word summary of your work, the technical category of submission; the type of submission (paper or poster); affiliations of all authors and contact information; and if you would like mentor support from an IRPS technical program committee member. A template for this [cover page](http://www.irps.org/tpc) is located at <http://www.irps.org/tpc>

Late Paper Submission: A limited number of late breaking news full length manuscripts will be considered on a space available basis. Completed manuscripts may be submitted until December 19, 2003. These manuscripts are to follow the criteria for accepted papers above. Accepted late papers will be included in the conference proceedings and in the technical presentations at the conference.

Electronic Submission Procedures: Please follow [electronic instructions](http://www.irps.org/tpc) on the IRPS Web page <http://www.irps.org/tpc>. Send electronic submissions to technical.chair@irps.org. All submissions will be acknowledged by e-mail within two weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair. If it is not possible to send your submission electronically, please contact the Technical Program Chair to make other arrangements.

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April 25-30, 2004 IRPS

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