

2010 IEEE INTERNATIONAL
RELIABILITY PHYSICS SYMPOSIUM
May 02 - 06, 2010 • Hyatt Regency Orange County • Anaheim, California
CALL FOR PAPERS and CALL FOR POSTERS

IRPS offers its attendees technical sessions, tutorials, workshops, a year-in-review seminar and a poster session, all covering state-of-the-art developments in the reliability physics of electronic and optoelectronic devices, materials, and systems. **Attendees returning from the IRPS will be better equipped to solve critical reliability problems and develop effective qualification procedures that affect their companies' bottom line.**

YOUR ORIGINAL PAPERS AND POSTERS ARE SOLICITED, which:

- A. Identify new or improve our understanding of the physics of failure and modeling of mechanisms in electronic and optoelectronic devices, materials, and systems;
- B. Identify how fabrication processes influence the susceptibility of product to particular physical failure mechanisms;
- C. Quantify the impact of device and circuit design, as well as material and process selection on reliability;
- D. Present new, innovative, or improved failure analysis techniques;
- E. Describe reliability testing/stressing, qualification, and screening methodologies or strategies for materials, devices, circuits, or chips; either at wafer- or module-level for commercial or "extreme" environments;
- F. Demonstrate techniques to build-in or extend reliability while meeting performance goals, especially as technologies are scaled.

For Silicon (Integrated Circuits, Discrete Devices, MEMS, TFTs), Compound Semiconductors & Optoelectronics (GaAs, GaN, LEDs, displays, photovoltaics), and emerging technologies including Organic Electronics and Nanotechnology IN THE FOLLOWING AREAS:

PRODUCT

Product Reliability and Burn-in – Product (Chip-level) Reliability Issues; New or Novel Failure Modes in Logic/Memory ICs; Burn-In Elimination Strategies; Wafer-level Burn-In; Correlation Between Yield, Infant Mortality, Burn-In Fallout, Technology Model Predictions
Non-volatile Memory – Unique Reliability Phenomena and Failure Mechanisms in Non-volatile Memories; Reliability of Ferroelectric, Magnetic, Phase Change, and Charge Trapping Memory Cells or Arrays
Qualification Strategies – New Techniques, Test Structures, and Product Vehicles for Technology of Chip Qualification; Best Practices to Reduce Cost and/or Time-to market; "Extreme" Environments (Temperature, Radiation, Humidity, etc); Best Practices for Fabless Semiconductor Companies
Circuits – Comprehending Reliability in Designs and Circuits; Physics of Soft Error Upsets; Analog Circuit Reliability Issues; Simulation/Modeling Techniques
Assembly and Packing – Package/Assembly Reliability; Stress Modeling, Cu and Low-k Issues, Chip Scale Integration, BGA and Flip Chip Assembly; Bump Reliability Issues
Failure Analysis – Evidence of New Failure Mechanisms; Failure Analysis Techniques; Case Histories
MEMS – Reliability of New Structures, Sensors, Actuators; Reliability Testing and Analysis of MEMS Systems, Design and Processing for Reliability

PROCESS

Device and Process – Reliability Driven Process Interactions; New Process-Related Reliability Issues and Associates Physics of Failure, including SI and NonSi based, OptoElectronics, MEMS, High Voltage Devices and Nanotechnology
Transistor – New Hot Carrier Phenomena; NBTI and PBTI; Transistor Scaling Issues; Impact of Alternative Gate Dielectrics; Effect of Materials' Degradation; Silicon on Insulator (SOI) Reliability Issues; High Performance Transistor Reliability; Mobility Enhancement Techniques such as Strained Si; Metal Gate Integration and TFT Devices
Interconnects – Defect and Wearout Phenomena in Cu and Al Systems; Low-k/Oxide Inter/Intra-Level Reliability; Mechanical Stress Related Reliability Issues; Joule Heating Effects; Modeling Mechanical & Thermal Behavior; Fast/Slow Stress Correlations
Device Dielectrics – Breakdown Mechanisms; New or Novel Dielectric Materials Reliability; Processing Interactions; Wearout Models; Gate Dielectric Thickness Scaling; Stress Methodologies; Multiple Dielectric Technologies
ESD and Latch-Up – Novel Structures including SOI and Bipolar; Damage Interpretation; Circuit/Process Improvements; Scaling Issues, RF CMOS
Process Induced Damage – Reliability Degradation Associated with Damage; Early Non-Destructive In-Line Detection and Reliability Analysis
Nanoelectronic Device Reliability – Drift & wear-out phenomenon associated with novel and future device structures including FINFET, carbon nanotube FET, semiconductor wire FET, molecular devices, and hybrid technologies.

NEW TECHNICAL FOCUS FOR IRPS 2010

IRPS 2010 is introducing a new technical topic on "**Reliability of Alternative Energy Technologies**" – Unique IC-based reliability phenomena and failure mechanisms in alternative energy technologies including solar, wind, transportation, nuclear, power transfer (smart grid) and power storage. Papers and posters which address the technical challenges of assuring product reliability for these emerging alternative energy technologies are solicited.

PAPER AND POSTER SUBMISSION INSTRUCTIONS

Abstracts Must Be Received By: OCTOBER 9, 2009

Abstract/Paper/Poster Submission: Your submission of original work should clearly and concisely state the specific results, why they are important, and how they relate to prior work. An on-line IRPS document template, located at <http://www.tpc.irps.org> is available and will save you time.

For papers: Only **two-page abstracts** will be accepted. Abstract submissions should include enough information to clearly indicate the path to develop a final paper. Full manuscripts of accepted papers will be due before the conference.

For posters: You may submit up to two pages. The technical committees reserve the right to accept paper submissions as posters.

For all submissions: Submit a 50 word summary of your work, the technical category of submission; the type of submission (paper or poster); affiliations of all authors and contact information.

Late Paper Submission: A limited number of late breaking news full-length manuscripts (*there is a 10-page limit with 6-pages being typical/optimal*) will be considered on a space available basis. Completed manuscripts may be submitted until **January 8, 2010**. Accepted late papers will be included in the conference proceedings and in the technical presentations at the conference.

NEW! ELECTRONIC SUBMISSION PROCEDURES: **Abstracts must be submitted electronically.** Do not email or mail hard copies to the conference office. Please read the paper preparation and submission guidelines before preparing your paper. Detailed submission instructions are on the IRPS Web page <http://www.irps.org>.

Technical Program Chair :

Ennis Ogawa, Technical Program Chair, 2010 IRPS
Broadcom Corporation
5300 California Avenue
Irvine, CA 92617 USA
Tel: +1-949-926-5507/Fax: +1-949-241-9240.
Email: etogawa1@yahoo.com

General Chair:

Thomas M. Moore, General Chair, 2010 IRPS
Omniprobe, Inc.
10410 Miller Road
Dallas, Texas 75238 USA
Tel: +1-214-572-6800/Fax: +1-214-572-6801
e-mail: moore@omniprobe.com

Awards: In addition to the Best & Outstanding Paper awards and the Best Poster award, IRPS will be presenting a Best Student Paper Award. To qualify for the student paper award, the IRPS presentation/poster must be given by a student and the first author must be that same student. Please indicate upon submission of an abstract if you would like to be considered for this award.