IRPS 2009 Program

TUESDAY MORNING
April 28, 2009

Plenary Session
Le Grand Salon, 8:00 am

1.1 A Development Alliance and Manufacturing Platform Business Model for Robust Chip Offerings, Michael Cadigan, IBM Systems &Technology Group, Development & Manufacturing General Manager: Semiconductor Solutions

Developing a state of the art technology begins by understanding the key attributes needed to be included in collaboration with both Customers and Development Alliance Partners. A Development Center that has the ability to fabricate and qualify every single feature within the new technology is critical to rapid development and implementation. A successfully qualified technology is a pre-requisite for subsequent products qualification. This includes a design kit that a broad set of customers can use to design either application-specific or foundry products. Product qualification must include evaluation of all aspects – technology, design and manufacturing – on both the reliability and functionality of the product in its intended application.

Early identification of the technology features is therefore paramount. In the model presented these decisions are reached by multi-company partners (a Development Alliance) working at every level, i.e. research, technology and process development, technology and circuit reliability analysis, and final integration into an industry standard design kit.

Technology Development Alliances deliver state-of-the-art technologies and design kits that can be implemented into foundry or ASIC products alike. Manufacturing Platforms using this model are then able to standardize product offerings within a single ecosystem. As a result, robust offerings are provided together with flexible manufacturing options within the platform.

1.2 **Assuring Microelectronic Component Reliability and Qualification – A Fabless Company's Perspective,** Robert Lutze, Vice President of Quality Assurance and Reliability at Broadcom Corporation

This paper reviews possible fabless models and how different the quality and reliability management may be among fabless companies. There are ASIC, turn key and pure foundry models used by different companies for different reasons. Each model involves different services provided by the foundry and require different engineering resources within the fabless company. Within the pure play foundry model, there are different terms and agreement in product procurement. They require strategies to achieve similar quality and reliability performance.

There may be wide spectrum among fabless companies in managing the product quality and reliability out of all these different procurement models. Using a single foundry is easier for Q&R management. However, it may not be desirable if the end customers require alternative foundry for back-up ensurance. Foundry selection and management will, then, be very important to ensure product quality and reliability for products across different foundries.

Each foundry may have its own quality and reliability management methodology and specification. Fabless companies need to use additional tools of gating the product quality if the Q&R goals provided by the foundry do not meet requirements. Fabless companies also need to assess whether the reliability monitor program provided by the foundry meets their need.

For pure play foundry, the fabless companies also need to manage other aspects of quality and reliability. This includes device package and assembly. The effort in managing the assembly quality is no less than managing the foundry quality. The fabless companies also need to have good ATE test strategy and product reliability program to ensure product quality and reliability.

TUESDAY AFTERNOON
April 28, 2009

Session 2A: Transistors: BTI and Traps
Le Grand Salon, 1:10 pm
Chair: Ben Kaczer, IMEC and Vice Chair: Jason Campbell, NIST

2A.1 (Invited) On the Temperature Dependence of NBTI Recovery (Paper Not Available), *Thomas Aichinger, Michael Nelhiebel, and Tibor Grasser*

Poly resistors can be used to perform fast in situ heating on a single device on wafer level. In our experiments we calibrate such a test structure and use it to generate a certain stress temperature during NBTI. During recovery the heater is switched off and the temperature is then defined by the underlying thermo chuck. By using this technique, our understanding of the recovery physics can be probed in an unprecedented manner.

2A.2 Unambiguous Identification of the NBTI Recovery Mechanism using Ultra-Fast Temperature Changes, *Thomas Aichinger, Michael Nelhiebel, and Tibor Grasser*

By making use of in situ heated test structures, we are able to perform fast temperature switches on single devices while keeping the device bias conditions untouched. In this paper we use the tool to vary the temperature in a defined way during stress and recovery. Additionally we also study the influence of gate bias switches at constant temperature. Our experiments indicate that recovery acceleration can be observed either by increasing the temperature or by switching the gate bias. Our observations suggest the neutralization of NBTI induced positive oxide traps by inelastic phonon-assisted tunneling to be the dominant recovery mechanism.

2A.3 Successful Measurements of Electron Energy Dependence of Interface-Trap-Induced Scattering in N-MOSFETs —Developed Hall Effect Measurements and Comparison with Theory, *Shigeki Kobayashi, Takamitsu Ishihara, Masumi Saitoh, Yukio Nakabayashi, Toshinori Numata, and Ken Uchida*

The dependence of the interface-trap-induced scattering on the electron kinetic energy (ε_{ele}) in nMOSFETs is investigated experimentally. The procedure to extract the accurate ε_{ele} dependence of the interface-trap-induced scattering relationship is developed based on the careful Hall effect measurements. As a result, it is demonstrated that as ε_{ele} increases, the interface-trap-induced scattering is suppressed more greatly than calculated by the conventional two-dimensional Coulomb scattering model. It is also found that the ε_{ele} dependence of the interface-trap-induced scattering is enhanced as D_{it} increases.

2A.4 Physics and Mechanisms of Dielectric Trap Profiling by Multi-Frequency Charge Pumping (MFCP) Method, *Muhammad Masuduzzaman, Ahmad Islam and Muhammad Alam*

MFCP is one of the most widely used, but least theoretically understood techniques to characterize bulk trap distribution in SiO_x/high-κ dielectric. In this work, we have developed a physically-based numerical framework and systematic back-extraction algorithm for widely used MFCP to show that back-extracted $N_T(x,E)$ reported in literature is often inaccurate, and sometimes misleading. We believe that only a coordinated analysis of L_{CH} dependent MFCP experiment within a theoretically justified MFCP algorithm, complemented with other methods, would allow unequivocal back-extraction of technologically critical $N_T(x,E)$ in the position-energy space within dielectric.

2A.5 Defect Profiling in the SiO_2/Al_2O_3 Interface using Variable T_{Charge}-$T_{Discharge}$ Amplitude Charge Pumping (VT^2ACP), *Mohammed Zahid, Robin Degraeve, Moonju Cho, Luigi Pantisano, Daniel.R Aguado, Jan Van Houdt, Guido Groeseneken, and Malgorzata Jurczak*

A Variable T_{charge}-$T_{discharge}$ Amplitude Charge Pumping (VT^2ACP) is used to profile defect in the SiO_2 and Al_2O_3 separately in *Flash Memory* based devices. It is shown that by independently controlling the pulse low timing "discharging time" and high level timing "charging time", the contribution of interface and bulk Al_2O_3 traps can be separated. By using the ellipsometry and the measured intersection time t_{charge} to trap in the high- k (~60 µs), SiO_2 thickness of 0.87 nm and scanning rate of 0.19nm/dec is found. Using a slanted wafer, the result shows that in the case of thin SiO_2 (~1nm) the trap density close to the substrate (short t_{charge}) is one order of magnitude higher compared to thick SiO_2 (~3nm). For t_{SiO2} = 1.7nm all traps are in the SiO_2 or SiO_2/Al_2O_3 transition layer. Only for the thickest SiO_2 layers (2.7 and 3 nm) the trap density becomes low and constant. Additionally WKB-approximation is used to calculate the filling probability of the traps (f_T), the modeled scanning rate nearly doubles to ~0.29 nm/dec and 0.27 nm/dec for amorphous and crystalline, respectively. In summary, the method of trap energy/depth profiling by using VT^2ACP allows scanning from ~0.5nm up to 1.2nm in depth and 0.1 to 0.7eV in energy range above the E_c^{Si} band depending on sample used. The results show that there exist significant interaction between SiO_2 and Al_2O_3 when processed with PDA 1000°C. For amorphous Al_2O_3 (PDA 700°C) the impact of the precursor is not reflected in the SiO_2 trap density while for crystalline Al_2O_3 no increase in trap density at 0.3eV above the E_c^{Si} band is observed.

Session 2B: Transistors: BTI and Traps

Le Grand Salon, 3:45 pm
Chair: Jason Campbell, NIST and Vice Chair: Ben Kaczer, IMEC

2B.1 A Unified Model for Permanent and Recoverable NBTI Based on Hole Trapping and Structure Relaxation, *Daniele Ielmini, Mariaflavia Manigrasso, Francesco Gattel, and Grazia Valentini*

Negative bias temperature instability (NBTI) strongly limits reliability of PMOS devices by degradation of threshold voltage, subthreshold slope and transconductance. The physical understanding of the NBTI mechanism is essential for searching paths of NBTI alleviation and providing realistic predictions for CMOS reliability. This work presents a new NBTI model based on hole trapping/detrapping accompanied by structural relaxation in the host dielectric. Simulations account for a time and T dependence of the drain current degradation during NBTI stress. Dynamic NBTI effects are then explained by alternative hole capture and emission during stress and relaxation stages. The impact of the activation energy dispersion on relaxation times is finally discussed.

2B.2 A Two-Stage Model for Negative Bias Temperature Instability, *Tibor Grasser, Ben Kaczer, Wolfgang Goes, Thomas Aichinger, Philipp Hehenberger, and Michael Nelhiebel*

Based on the established properties of the most commonly observed defect in amorphous oxides, the *E*_ center, we suggest a coupled two-stage model to explain the negative bias temperature instability. We show that a full model that includes the creation of *E*_ centers from their neutral oxygen vacancy precursors and their ability to be repeatedly charged and discharged prior to total annealing is required to describe the first stage of degradation. In the second stage a positively charged *E*_ center can trigger the depassivation of *P*b centers at the Si/SiO2 interface or *K*N centers in oxynitrides to create an unpassivated silicon dangling bond. We evaluate the new model to experimental data obtained from three vastly different technologies (thick SiO2, SiON, and HK) and obtain very promising results.

2B.3 Systematic Study of the Relationship Between 1/f noise, Interface State Defects and Mobility Degradation of High-K /Metal CMOSFETs on (110) And (100) Substrate, *Motoyuki Sato, Takayuki Aoyama, Yasuo Nara, and Yuzuru Ohji*

We investigated the relationship between the 1/f noise, carrier mobility and interface state defects between the Si substrate and oxide on (110) and (100) substrates. In the case of pMOSFETs, the 1/f noise is independent of the mobility degradation due to the increase of effective hole mass. However, the 1/f noise is strongly related to the degradation in the hole mobility due to the process integration damage. With hole mobilities becoming lower, 1/f noise intensity was enhanced. On the other hand, the 1/f noise of nMOSFETs is rerated to interface defects rather than electron mobility degradation. Additionally its behavior was affected by the difference between Pb0 and Pb1.

2B.4 Investigation of Post-NBT Stress Current Instability Modes in HfSiON Gate Dielectric pMOSFETs by Measurement of Individual Trapped Charge Emissions, *Huan-Chi Ma, Jung-Piao Chiu, Chun-Jung Tang, Tahui Wang, and Chih-Sheng Chang*

Bipolar charge detrapping induced current instability in HfSiON gate dielectric pMOSFETs after negative bias and temperature stress is studied by using a fast transient measurement technique. Both single electron and single hole emissions are observed, leading to post-stress current degradation and recovery, respectively. The NBT stress voltage and temperature effect on post-stress current evolution is explored. Clear evidence of electron and hole trapping in NBT stress is demonstrated. A bipolar charge trapping/detrapping model and charge detrapping paths based on measured charge emission times are proposed.

2B.5 NBTI from the Perspective of Defect States with Widely Distributed Time Scales, *Ben Kaczer, T. Grasser, J. Martin-Martinez, E. Simoen, M. Aoulaiche, Ph.J. Roussel, G. Groeseneken*

Broad similarity between negative bias temperature instability (NBTI) relaxation and 1/f noise is observed. Individual transitions in NBTI relaxation in small pFETs are observed and Poisson defect number statistics is inferred. Finally, it is argued that the wide distribution of defect times should be considered in addition to defect number variation in small devices.

SESSION 2C: Compound Transistors

Marquette Room, 1:10 pm

Chair: Gaudenzio Meneghesso, University of Padova and

Vice Chair: Brian Skromme, Arizona State University

2C.1 (Invited) Reliability of GaN HEMTs: Current Status and Future Technology, *Toshihiro Ohki, Toshihide Kikkawa, Yusuke Inoue, Masahito Kanamura, Naoya Okamoto, Kozo Makiyama, Kenji Imanishi, Hisao Shigematsu, Kazukiyo Joshin, and Naoki Hara*

In this paper, we describe highly reliable GaN high electron mobility transistors (HEMTs) for high-power and highefficiency amplifiers. First, we present the reliability mechanisms and progress on the previously reported GaN HEMTs. Next, we introduce our specific device structure for GaN HEMTs for improving reliability. An n-GaN cap and optimized buffer layer are used to realize high efficiency and high reliability by suppressing current collapse and quiescent current (*Idsq*)-drift. Finally, we propose a new device process around the gate electrode for further improvement of reliability. Preventing gate edge silicidation leads to reduced gate leakage current and suppression of initial degradation in a DC-stress test under hightemperature and high-voltage conditions. Gate edge engineering plays a key role in reducing the gate leakage current and improving reliability.

2C.2 Influence of GaN Cap on Robustness of AlGaN/GaN HEMTs, *Ponky Ivo, Arkadiusz Glowacki, Reza Pazirandeh, Eldad Bahat-Treidel, Richard Lossy, Joachim Würfl, Christian Boit, and Günther Tränkle*

DC-Step-Stress-Tests of GaN HEMTs have been performed on wafers with and without GaN-cap. The tests consist of a step ramping of drain-source voltage V_{DS} by 5V every two hours at off-state. The irreversible evolution of leakage current starting at a certain drain voltage has been taken as a criterion for the onset of device degradation. It has been stated that there is a stability limit for V_{DS} depending on the epitaxial design. It has been found that wafers with GaN cap show much higher critical voltages as compared to non-capped epitaxial designs. Electroluminescence measurements have been performed to localize defects after DC-Step-Stress-Tests up to 80V for wafer without GaN cap and 120V for wafer with GaN cap.

2C.3 Reliability Review of 250 GHz Fully Self Aligned Heterojunction Bipolar Transistors for Millimeter-Wave Applications, *Malick Diop, Mathieu Marin, Nathalie Revil, Franck Pourchon, Cedric Leyris, Pascal Chevalier, and Gérard Ghibaudo*

Reliability performances of fully self aligned heterojunction bipolar transistors were investigated under high current and voltage stress conditions. We point out in this paper that Generation-Recombination traps induced by reverse bias stress can be repaired by forward bias. This is possible thanks to high enough device temperature (strong self-heating condition). Low frequency noise measurements and HICUM modelling of power dissipation refine this analysis. Finally, degradation of base–collector junction was investigated under mixed–mode stress and reveals a predominance of defects induced in the space charge area by impact ionization.

2C.4 Mixed-Mode Stress Degradation Mechanisms in pnp SiGe HBTs, *Partha Chakraborty, Aravind Appaswamy, Prabir Saha, Nand Jha, John Cressler, Hiroshi Yasuda, Bob Eklund, and Rick Wise*

This study investigates the high-voltage/high-current mixed-mode stress-induced damage mechanisms of pnp SiGe HBTs. Different accelerated stress methods were applied to pnp SiGe HBTs from a complementary-SiGe BiCMOS process technology. The damage mechanisms from mixed-mode stress are identified and experimental proof of the type of hot carriers responsible for the observed mixed-mode stress damage is presented. Detailed TCAD simulations were performed to validate the physical location of the mixed-mode stress damage observed in this study.

Session 2D: Opto-Electronics and Thin Films

Marquette Room, 2:55 pm
Chair: Gaudenzion Meneghesso, University of Padova and
Vice Chair: Glenn Alers, University of California, Santa Cruz

2D.1 (Invited) Reliability Issues in AlGaN Based Deep Ultraviolet Light Emitting Diodes, *Asif Khan, Seongmo Hwang, Jonathan Lowder, Vinod Adivarahan, and Qhalid Fareed*

AlGaN based deep ultraviolet light emitting diodes (DUV LEDs) are key components in systems for air, water, and food purification and germicidal applications. Because of the heteroepitaxial growth of the DUV LED epilayers on sapphire, they have a large number of dislocations that invariably leads to a reduction of quantum efficiency and lifetime degradation. In this paper, we present our recent work at developing DUV LEDs with different device geometries, which includes a new micro-pixel electrode arrangement. This arrangement was used to study mechanisms responsible for their degradation. The micro-pixel device geometry with some new packaging schemes led to DUV LEDs with emission at 280 nm and lifetimes well in excess of 3000 hours. In this paper experimental details and the results of our study are presented.

2D.2 Degradation Mechanisms Beyond Device Self-Heating in Deep Ultraviolet Light Emitting Diodes, *Craig Moe, Meredith Reed, Gregory Garrett, Grace Metcalfe, Troy Alexander, Hongen Shen, Michael Wraback, Alex Lunev, Yuriy Bilenko, Xuhong Hu, Ajay Sattu, Jianyu Deng, Maxim Shatalov, and Remis Gaska*

Lifetime measurements on single, packaged UV LEDs were performed under constant current injection at 20 and 75 mA (60 and 226 A/cm2). The junction temperature at operation was found by micro-Raman spectroscopy to be 57 and 184 ◦C, respectively. Unbiased LEDs of similar characteristics placed in an oven baked at the equivalent operating junction temperatures showed a degradation in output power similar to that in the current injection devices during the initial 24 hours, but did not continue to degrade beyond that time. These studies imply that device heating, is correlated with the initial drop in output power during burn-in, but is not directly linked to the total degradation over the lifetime of the device. Time-resolved PL studies on the device active region as well as further electro-optic measurements indicate that the degradation is not due primarily to that of the active region, but may be associated with generation of point defects such as N-vacancies near the *p-n* junction.

2D.3 Thermally Activated Degradation and Package Instabilities of Low Flux LEDs, *L. Trevisanello, F. De Zuani, M. Meneghini, N. Trivellin, E. Zanoni and G. Meneghesso*

The results achieved in an accelerated life-time test on Phosphor-Converted Light Emitting Diodes (PC-LEDs) have been reported. Two different families of commercially available low-flux devices have been widely characterized and a comparative analysis on performances has been carried out. A wide set of devices has been submitted to a combined electrothermal accelerated stress under different aging conditions. The stress induced a luminous flux decay on LEDs from both series. In particular, the lumen decay was found to be thermally activated for one set of devices. The aged devices showed also a degradation of chromatic properties, in terms of a blue or yellow shift for the two different families. The failure modes found have been detected also in devices aged at constant temperature and no bias. The degradation mechanism responsible for lumen decay and chromatic shift was ascribed to the thermally activated package instabilities. A failure analysis has been carried out on failed devices, detecting different failure modes related to the package (chip detachment) and to the chip (generation of low impedance paths that shorted the junction).

2D.4 (Invited) Reliability and Lifetime of Flexible Organic Electronics, *Melissa Kreger, Eitan Ziera, Bob Eckert, Steve Lee, Bob Pusateri, Steve Wicks, Shiela Rodman, Jens Hauch, and Christoph Brabec*

We will introduce a flexible, lightweight organic thin film device. Coating and printing technology are used to build up various layers onto a PET substrate. There is one transparent electrode, a series of active layers, and an opaque silver electrode. The photovoltaic device is sensitive to oxygen and water. The module is packaged on the front and back with a laminate that acts as a barrier to the environment. The exterior layer of the package contains a UV blocker to prevent yellowing and cracking of the plastic and degradation of the semiconductor. The main challenges are achieving the required barrier properties of the packaging at relatively low cost. The critical factors for the laminate film and the adhesive are water vapor transmission rate (WVTR) and oxygen transmission rate (OTR) through the top and bottom of the package and ingress through the edges. We will discuss the current barrier film performance with respect to necessary improvements and stability of barrier properties under extreme conditions. In this paper we will define reliability testing for organic thin film flexible photovoltaics. We will give examples of accelerated lifetime testing (ALT) protocols designed to quantify materials with respect to product specification and to meet customer needs. We will show the correlation between various standardized accelerated testing conditions and discuss progress in packaging. We find examples of ALT used in the solar industry and organic light emitting display technology and discuss how those might be structured to address the uniqueness of flexible electronics. With the standard being set by glass, some of the standard ALT might be modified to provide a meaningful evaluation of flex. In conclusion, we will present and discuss some common failure mechanisms, show evidence of degradation within the package and explore how this compromises photovoltaic performance.

2D.5 Improved Reliability of Organic Light-Emitting Diodes with Indium-Zinc-Oxide Anode Contact, *Alessandro Pinato, Matteo Meneghini, Andrea Cester, Nicola Wrachien, Augusto Tazzoli, Enrico Zanoni, Gaudenzio Meneghesso, and Brian D'Andrade, J. Esler, S. Xia, J. Brown*

We report a comparison of the performance and reliability of Organic Light-Emitting Diodes with Indium-Tin Oxide and Indium-Zinc Oxide anode layer. The devices have been compared in terms of efficiency, thermal resistance and reliability. The results of this analysis indicate that: *(i)* the use of an IZO anode allows to achieve an efficiency comparable to the case of ITO contacts; *(ii)* devices with IZO contact have a lower thermal resistance, compared to the ones with ITO anode; *(iii)* OLEDs with IZO anode exhibit an higher reliability. The use of IZO anodes allows a better heat dissipation and devices reliability.

2D.6 Threshold Voltage Instability in Organic TFT with SiO_2 and SiO_2/Parylene-Stack Dielectrics, *Nicola Wrachien, Andrea Cester, Alessandro Pinato, Matteo Meneghini, Augusto Tazzoli, Gaudenzio Meneghesso, Jaroslav Kovac, Jan Jakabovic, and Daniel Donoval*

We study the charge trapping/detrapping kinetics on pentacene-based organic thin-film-transistors featuring SiO_2 and SiO_2/parylene C stack gate insulators. The threshold voltage variation is correlated with the gate pulse width and amplitude, and it is due to charge trapping, rather than permanent degradation. The detrapping kinetics is thermally-activated and it is accelerated if the device is illuminated. The additional parylene layer brings benefits by strongly reducing the charge trapping/detrapping, and increasing the hole mobility and the drain current.

2D.7 Life-Stress Relationship for Thin Film Transistor Gate Line Interconnects on Flexible Substrates, *Thomas Martin and Aris Christou*

Change in resistance of interconnect traces on flexible substrates is dependent on material properties and mechanical stress imposed by tensile strain. Dedicated test structures and a mechanical flexing / data collection system were designed and fabricated to collect time to failure data based on cyclic loading to different radii of curvature. We propose a life-stress model based on an inverse power law relationship defining the characteristic life of a Weibull life distribution.

Session 2E: Novel Memories

Jolliet Room, 1:10 pm

Hanmant Belgal, Intel and Vice Chair: Hang-Ting Lue, Macronix

2E.1 Statistical and Scaling Behavior of Structural Relaxation Effects in Phase-Change Memory (PCM) Devices, *Mattia Boniardi, Daniele Ielmini, Simone Lavizzari, Andrea Lacaita, Andrea Redaelli, and Agostino Pirovano*

The phase-change memory (PCM) technology represents one of the most attractive concepts for next generation data storage. PCM behavior is mainly limited by the structural relaxation (SR) and by the crystallization of an amorphous chalcogenide material: the ternary alloy *Ge*2*Sb*2*Te*5. SR is a local structural-rearrangement at the atomic/bonding scale and crystallization is the reaching of a periodic atomic structure. While the retention capabilities related to crystallization have been already extensively addressed in the literature, both at the single-cell and at the statistical level, those related to SR have been mainly studied at the intrinsic level and a statistical analysis at the device level is still lacking. The purpose of this paper is to study the statistical and scaling behavior of the SR phenomenon in PCM devices, through experimental and modeling tools, allowing for long term, physics-based, reliability extrapolations in large-scaled PCM arrays.

2E.2 A New Automated Methodology for Random Telegraph Signal Identification and Characterization: A Case Study on Phase Change Memory Arrays, *Andrea Chimenton, Cristian Zambelli, and Piero Olivo*

We present a new method for statistical analysis of Random Telegraph Signals. Simulations show good features of the method which is a powerful tool for evaluating the impact of RTS on performance and reliability of electron devices. Its application to Phase Change Memories will be discussed in order to successfully analyze a new RTS phenomenon observed in the SET state during cycling. The physical nature of the phenomenon has been related to random presence of extra Parasitic Crystal (PC) path in the active volume of the chalcogenide material. The analysis shows also that the PC is correlated with the anomalous tail of RESET distribution.

2E.3 Effect of ReRAM-Stack Asymmetry on Read Disturb Immunity, *Masayuki Terai, Setsu Kotsuji, Hiromitsu Hada, Noriyuki Iguchi, Toshinari Ichihashi, and Shinji Fujieda*

We investigated the effect of ReRAM-stack asymmetry on read disturb immunity. Stacking stoichiometric Ta_2O_5 and ultrathin TiO_2 led to bipolar switching property. Filament (conduction path) penetrated both Ta_2O_5 and TiO_2 layer. Because single Ta_2O_5 film has no switching property, the resistance was not changed under positive bias on Ta_2O_5-side electrode. Under negative bias, the resistance of the filament near TiO_2-side electrode increases because of anodic oxidation. A high read-disturb immunity were achieved by using the 1T1R ReRAM of this stack. These results can be attributed to the asymmetric switching behavior of the stoichiometric Ta_2O_5/ultrathin-TiO_2 stack.

2E.4 A Study of Dielectric Breakdown Mechanism in CoFeB/MgO/CoFeB Magnetic Tunnel Junction, *Chikako Yoshida, Masaki Kurasawa, Young Min Lee, Koji Tsunoda, Masaki Aoki, and Yoshihiro Sugiyama*

We examined the breakdown characteristics of a 1-nm-thick MgO barrier by measuring the time dependent dielectric breakdown (TDDB) and conducting atomic force microscopy (C-AFM) observation. We found that two different local conduction modes, the percolation path and Fowler-Nordheim (F-N) tunneling, contribute to dielectric breakdown. Furthermore, the operating voltage of magnetic tunnel junctions (MTJs) for maintaining reliability over ten years against dielectric breakdown was discussed.

Session 2F: Assembly and Packaging
Jolliet Room, 4:10 pm
Chair: Richard Blish, Spansion

2F.1 Withdrawn

2F.2 Electromigration Behavior of Micro Sn Bump Under Pulsed DC, *Ha-Young You, Byoung-Joon Kim, and Young-Chang Joo*

Pulsed electromigration (EM) was performed for flip-chip solder bump. Pulsed EM was conducted with current density of $5.2 \sim 7.1 \times 10^4$ A/cm^2 at 160 ^{o}C. DC EM was also performed at $3.6 \sim 4.7 \times 10^4$ A/cm^2 for comparison. The life times of pulsed EM samples are larger than those of DC EM samples. The current density exponent for 1Hz pulsed EM is 1.42 and that of DC EM is 2.25. The life time of pulsed EM was successively converted into that of DC EM by considering Joule heating temperature. Failure time of pulsed EM increases with increasing frequencies around 2 Hz

2F.3 Comparison of Electromigration Behaviors of SnAg and SnCu Solders, *Minhua Lu, Da-Yuan Shih, Charles Goldsmith, and Thomas Wassick*

Two commonly used Pb-free solders, SnAg and SnCu, are studied for electromigration (EM) reliability. Two major EM failure mechanisms are identified in Sn-based Pb-free solders, which is mainly due to the differences in microstructures and Sn-grain orientation. In general, the EM damage in SnCu solder is driven by the fast interstitial diffusion of Ni and Cu away from solder/UBM interface and leads to early fails; while the damage in SnAg solders is mostly dominated by Sn-self diffusion resulting in longer lifetime. The effective activation energy is 0.95 eV for SnAg solder and 0.54 eV for SnCu solder. The current density power law exponent is 2 for SnAg and 1.2 for SnCu, respectively. Blech effect is observed in the solders with Sn-self diffusion dominated failures. The roles of Ag and Cu on EM performance will be discussed.

2F.4 (Invited) Package Design and Material Impact on Board Level Reliability of Fine Pitch Packages, *Ahmer Syed*

The reliability of an electronic package is ultimately determined by the environment and application in which it is used. Due to the proliferation of electronic devices across market segments ranging from automotive to small, hand-held devices, electronic packages experience different loading conditions and thus need to pass varying reliability requirements. The gradual migration to Pb free, RoHS, and Green packaging in various sectors of the industry is further challenging the manufacturers of Electronic Packages to provide reliable solutions with diverse material sets. As the package shrinks and pin count grows, package design and materials play key roles in determining the board level performance. Mold compound, ball pad surface finish and ball composition are considered key materials influencing board level reliability. Package design features such as mold cap thickness, solder mask opening, ball size, die size as well as the presence of a ball or bump also affect the drop, bend, and temperature cycling performance for a given package size. The best material/construction combination for drop performance is not necessarily the best combination for optimum bend and temperature cycle reliability. This paper presents a collection of test data showing how a choice of one factor (design or material) can have a different effect on performance depending on the loading conditions.

2F.5 (Invited) Process Integration Considerations Towards 300 mm TSV Manufacturing-Moving Beyond the Champion SEM, *Sesh Ramaswami*

Through-silicon via (TSV) will transition to high volume production when end-customer value (as exhibited by functionality, performance, form factor, etc) are delivered at equivalent yield and cost. While this has been successfully achieved for CMOS image sensors (starting with 200mm), significant work remains to be done in the TSV value chain (design-materials-process-packaging-test) in the communication and memory segments. This talk will address key unit process/process integration challenges and highlight recent internal/ partner and industry findings in the context of TSV manufacturability at 300 mm.

Session 2G: Extreme Environments
Duluth/Mackenzie Rooms, 1:10 pm
Chair: Hugh Barnaby, Arizona State University and
Vice Chair: Bert Vermeire, Arizona State University

1:15 pm
2G.1 Impact of Deep Trench Isolation on Advanced SiGe HBT Reliability in Radiation Environments, *Stanley Phillips, Akil Sutton, Aravind Appaswamy, Marco Bellini, John Cressler, Alex Grillo, Gyorgy Vizkelethy, Paul Dodd, Mike McCurdy, Robert Reed, and Paul Marshall*

We investigate, for the first time, the impact of deep trench isolation on the TID and SEU tolerance of advanced SiGe HBTs. We employ a combination of 63 MeV protons, 10 keV X-rays, and 36 MeV oxygen ion microbeam irradiation and compare a 3rd generation, high-performance (HP), deep-trench isolated, SiGe BiCMOS platform with its cost-performance (CP) variant without deep-trenches. Although the CP SiGe HBTs are shown to be more susceptible to TID damage, they are also surprisingly found to offer a potential built-in self-mitigation mechanism for SEU. Calibrated, full 3-D ion strike TCAD simulations are employed to explain the results.

2G.2 Analytical Expression for Temporal Width Characterization of Radiation-Induced Pulse Noises in SOI CMOS Logic Gates, *Daisuke Kobayashi, Takahiro Makino, and Kazuyuki Hirose*

Radiation-induced pulse noises called single-event transients, SETs, are becoming a serious soft-error source for logic VLSIs. Analytical models explicitly expressing the relationship between the pulse width and radiation/device/circuit parameters are desired as guidelines to develop optimized countermeasures. A simple mathematical expression is devised for characterizing SET pulse widths in SOI CMOS technologies. It is based on the physical mechanisms of the SETs and on the idea of Moll's storage time. Device simulations demonstrate that the expression explains pulse-width trends properly for large radiation-induced noise charges.

2G.3 The Effect of Elevated Temperature on Digital Single Event Transient Pulse Widths in a Bulk CMOS Technology, *Matthew Gadlage, Jon Ahlbin, Balaji Narasimham, Vishwa Ramachandran, Cody Dinkins, Bharat Bhuva, Ronald Schrimpf, and Robert Shuler*

One of the major factors affecting soft-error rates is single-event transient (SET) pulse widths. In this work, heavy-ion induced SET pulse widths are reported at temperatures ranging from 25° to 100° C with an autonomous SET capture circuit. Experimental and simulation results in a 90-nm bulk CMOS technology indicate an increase as high as 37% in average SET pulse width with increasing operating temperature, with some pulses almost 2 ns long at higher temperatures. The increase in the SET pulse width can be explained by the dependence of bipolar amplification on temperature.

2G.4 Reliability of High Performance Standard Two-Edge and Radiation Hardened by Design Enclosed Geometry Transistors, *Michael McLain, Hugh Barnaby, Ivan Esqueda, Jonathan Oder, and Bert Vermeire*

It was recently shown that radiation hardened by design (RHBD) annular-gate MOSFETs not only provide totaldose radiation tolerance, but can also improve the hot-carrier reliability of advanced CMOS circuits. In this paper, the hotcarrier reliability of standard two-edge and enclosed geometry transistors intended for use in space and strategic environments is demonstrated. Hot-carrier reliability measurements on standard two-edge, standard enclosed, gate under-lap enclosed, and annular transistors fabricated in the same 90 nm high performance technology indicate an improvement in hot-carrier lifetime in the enclosed geometry and multi-finger transistor designs when compared to a conventional single stripe MOSFET. Two-dimensional device simulations, along with experimental measurements, provide physical insight into the reliability response of each device type.

2G.5 (Invited) Improvised Explosive Device (IED) Counter-Measures in Iraq, *James Ziegler*

Land mines have been used in warfare since the 13th century. Their greatest weakness has always been to coordinate the timing of the explosion with an enemy's movement. Improvised Explosive Devices (IED's) are mines that are constructed in the field using available munitions. In the 16th century these were detonated using a clock-timer or concealed trip-wire. Remote RF-controlled IED's were first used in 1984, using a model airplane controller. The modern car fob, which allows remote opening

of car doors, was invented in 1996, and rapidly became ubiquitous. However, it was unanticipated that it would rapidly become the heart of a major weapons system, commonly called a RF-IED. IED's currently cause more than 70% of the U.S. casualties in Iraq. The use of RF-IED's allows the IED to be controlled up to several miles away (using a cell phone) and allows accurate timing of the detonation. New research is beginning to point to ways to deactivate the IED RF electronic controls without detonation of the explosives, using particle radiation (soft fails). Experiments with many types of radiation have shown remarkable effects, which are not well understood. This talk will review the use of IED's in Iraq, and the new counter-measures being studied.

Session 2H: Soft Errors

Duluth/Mackenzie Rooms, 3:45 pm

Chair: Charles Slayman, Sun and Vice Chair: Norbert Seifert, Intel

2H.1 (Invited) NSEU Impact on Commercial Avionics, *David Matthews and Michael Dion*

Neutron Single Event Upsets (NSEU) are known to have a significant impact on modern IC's used in typical ground applications. The impact is orders of magnitude more frequent and critical when IC's are used in avionics flying at 40,000 ft due to the higher atmospheric neutron flux and the potential for critical impact to human safety. As ICs become more sensitive and as systems use more bits, the systems become more sensitive. Avionics manufacturers use a variety of methods to manage the effects of NSEU, starting in design, through the product assessment process, and into the extended field life of products.

2H.2 Single-Event Effects on Ultra-Low Power CMOS Circuits, *Megan Casey, Bharat Bhuva, Sarah Nation, Oluwole Amusan, T. Daniel Loveless, Lloyd Massengill, Dale McMorrow, and Joseph Melinger*

Operating circuits in the subthreshold region is a simple method to lower total power consumption. The lower supply voltages decrease the electric fields present in the devices (resulting in lower charge collection), but increase the time required to remove these charges. These two competing mechanisms are characterized through two-photon absorption experiments for single-events to show that single-event vulnerability does not show a linear relationship with power supply voltage, as would be expected, in the subthreshold region. Single-event characterization is carried out using higher harmonic oscillation in ring oscillators with large numbers of stages over a wide range of supply voltages.

2H.3 Comparison of Alpha-Particle and Neutron-Induced Combinational and Sequential Logic Error Rates at the 32nm Technology Node, *Balkaran Gill, Norbert Seifert, and Victor Zia*

We report on particle induced upset rates of combinational and sequential logic. A novel test chip has been designed in a 32nm process to study the effects of single event transients (SET) and to verify the accuracy of our simulation models. The test chip has been tested under neutron and alpha particle radiation. Our measured data verify simulation-based projections that while static logic at the 32nm technology node is sensitive to both alpha particle and neutron radiation, it is not a dominant contributor at the chip-level.

2H.4 Alpha Particle and Neutron-Induced Soft Error Rates and Scaling Trends in SRAM, *Hajime Kobayashi, Nobutaka Kawamoto, Jun Kase, and Ken Shiraish*

We performed underground real-time tests to obtain alpha particle-induced soft error rates (α-SER) for SRAMs, and the α-SER was compared to the neutron-induced soft error rate (n-SER) obtained from accelerated tests. As devices are scaled down, the α-SER increased while the n-SER slightly decreased. The α-SER could be greater than the n-SER in 90 nm technology even when the ultra-low-alpha grade was used for package resin. Simulation results suggested that the α-SER decreased from 65 nm technology while the n-SER increased from 45 nm technology due to direct ionization from protons generated in the n + Si nuclear reaction.

2H.5 An Industrial Fault Injection Platform for Soft-Error Dependability Analysis and Hardening of Complex System-On-a-Chip, *Jean-Marc Daveau, Alexandre Blampey, Gilles Gasiot, Joseph Bulone, and Philippe Roche*

This paper presents a fault injection platform that is currently developed and used to perform soft-error dependability analysis and hardening of complex SoCs1. Primarily, it is oriented toward safety analysis, safety requirement conformance testing and hardening of complex SoCs. This platform makes use of clusters of hardware emulation resources available for SoC verification to achieve massive faults injection capabilities. It is able to distribute fault injection campaigns across multiple heterogeneous emulation platforms to achieve high fault coverage. It is able to virtually handle almost any circuit size and is designed to support all kind of designs. We present the first results obtained on a small design, the Leon2 IP, on which exhaustive fault injection have been performed.

2H.6 (Invited) Qualification Issues and Pitfalls for Advanced Semiconductor Devices in Space, *David Sunderland*

Increasing satellite performance within size, weight and power constraints demands access to advanced semiconductors, yet environmental, reliability and schedule requirements remain. Successful technology insertion requires knowledge of failure mechanisms, design limitations and screening flow. We review Boeing's approach, critical issues and potential pitfalls, illustrated by experience with IBM ASIC technology.

WEDNESDAY MORNING
April 29, 2009

Session 3A: Fabless and Foundry Qualification

Le Grand Salon, 8:15 am
Chair: Shi-Jie Wen, Cisco and Vice Chair: Sriram Kalpat, Qualcomm

3A.1 (Invited) Reliability Framework in a Fabless-Foundry Environment, ***Sheng****-Yueh (S.Y.) Pai, J. K. Jerry Lee, Kenny Ng, Ching-Heng (Reality) Hsiao, K. C. Su, and Erh-Nan Chou*

An integrated and collaborative framework is presented to address the reliability challenges faced in a fabless-foundry environment. Through design-for-reliability, proper process standardization, defect density reduction and electrical screening, reliability of the highest level has been achieved in FPGA devices suitable for not only commercial, but also automotive and aerospace applications.

3A.2 Advanced Process & Product Reliability Development in Fabless Environment, *Gautam Verma, Kenneth Wu, Bruce Euzent, and Cheng Huang*

In this paper, we discuss the methodology used between a foundry and a fabless FPGA component supplier for ensuring a high yielding, reliable FPGA product at an advanced technology node. It is shown that close collaboration between the fabless supplier and foundry in technology development and manufacturing is essential for success. We discuss historical reliability trends as well as reliability data from the latest 40nm technology, which today is the most advanced technology node for a FPGA in production.

3A.3 (Invited) Qualification & Reliability Monitoring for Small Quantity ASIC Populations, *David Alexander, Stephen Philpy, and Donald Pierce*

The authors present a discussion of the issues and an approach for qualification and reliability monitoring for small quantity ASICs used in long lifetime applications. Special attention is given to issues associated with sub-100 nm technologies and the unique challenges posed by new materials and processes.

3A.4 A Complete and Automatic Advanced Model Verification Platform for 32nm Technology and Beyond, *Yanfeng Li, Riko Radojcic, Mark Nakamoto, Juzer Fatehi, Geng Zhang, Xisheng Zhang, Jinfeng Kang, Xiaolang Yan, and Yan Wang*

Variability from different sources such as layout-dependent effect has been a main obstacle against aggressive design rule and shrinking corner margins in 45nm node and beyond. This paper reports and demonstrates a verification platform to qualify the advanced models that address variability including layout-dependent reliability effects. This verification platform has been successfully used in real design exercise at 45nm technology and is being applied for 32nm technology. Test structures and methodologies of verifying different variability-aware models are presented. The platform was demonstrated to be flexible enough to account for new layout-dependent reliability behaviors in STRAIN technology.

Session 3B: Product Qualification

Le Grand Salon, 10:25 am

Chair: Carole Graas, IBM

3B.1 Reliability of Thyristor-Based Memory Cells, *Craig Salling, Kevin Yang, Rajesh Gupta, Dennis Hayes, Janice Tamayo, Vasudevan Gopalakrishnan, and Scott Robins*

This is the first published study of the reliability of Thyristor-based memories. Thyristor test structures indicate that the reliability lifetime of a nominal bit is 1.0E4 yrs. 9Mb and 18Mb test chips yield array reliability results for HTOL (37 FIT), SER (610 FIT/Mb), and X-rays (max dose > 450rad).

3B.2 Improved Integrated Circuits Qualification using Dynamic Laser Stimulation Techniques, *Amjad Deyine, Kevin Sanchez, Philippe Perdu, Fabien Battistella, and Dean Lewis*

Dynamic Laser Stimulation techniques have been developed with success for failure analysis of integrated circuit subjected to "Soft Defect". Weakness in design and physical defect can be isolated and located through these methodologies for digital, analog and mixed mode devices. But they are now successfully used embedded in qualification process since they provide accurate information about the device robustness and weaknesses evolutions. Efficiency of this approach has been demonstrated on an EEPROM.

3B.3 Compensation of Operation-Related F_{MAX} Degradation by Adaptive Control of Circuit Operating Voltage, *Maciej Wiatr, Richard Heller, Jan Hoentschel, Rolf Geilenkeuser, Stephen Wong, Vishal Shah, Tilo Mantei, Martin Majer, Ekkehard Pruefer, Casey Scott, Tom Rodes, Karsten Wieczorek, M. Horstmann, and David Greenlaw*

The impact of HCI and NBTI on device DC, Ring Oscillator (RO) AC as well as on the degradation of product operating frequency (FMAX) has been extensively studied. We have developed a method, which allows the compensation of HCI/NBTI-related device and product performance degradation by adaptive control of operating voltage and power for the integrated circuit. Depending on the constraints applied to the product reliability and power, full or partial performance compensation is possible applying our new approach. The win in guard bands and thus a product classification advantage is demonstrated on one of our high-performance microprocessors.

3B.4 (Invited) Emerging Post-CMOS Switch Options-A Product Reliability Perspective, *Kerry Bernstein*

Sooner or later, CMOS Scaling will come to an end. What do we do next? A number of very different switches have been proposed as replacements, some of which in fact do not even use electron charge as the state variable. Instead, these switches pass tokens in the Spin, Excitonic, Photonic, magnetic, qubit, or heat domains. The emergent physical behaviors and idiosyncrasies of these novel switches can compliment the execution of specific task algorithms or workloads, and improve overall thru-put in high performance computing. They also present new reliability challenges and perils, however. This talk will describe some of these potential CMOS replacements, how they may be used in design, and the concerns they raise for those who manage product reliability.

SESSION 3C: Flash Memory

Marquette/Jolliet Rooms, 8:15 am

Chair: Hang-Ting Lue, Macronix and Vice Chair: Hanmant Belgal, Intel

3C.1 Granular Electron Injection and Random Telegraph Noise Impact on the Programming Accuracy of NOR Flash Memories, *Christian Monzio Compagnoni, Luca Chiavarone, Marcello Calabrese, Riccardo Gusmeroli, Michele Ghidotti, Andrea L. Lacaita, Alessandro S. Spinelli, and Angelo Visconti*

This work investigates charge-granularity effects during CHE programming of NOR Flash memories, comparing granular electron injection and RTN limitations to the accuracy of the programming algorithm. The spread of the V_T shift determined by the electron injection statistics is studied as a function of the CHE programming conditions, explaining the results by a model accounting for the sub-poissonian electron transfer to the floating gate. The scaling trend of the injection spread is investigated on NOR technologies from 180 to 45nm and its contribution to the width of the V_T distribution in presence of a program verify is separated from that given by RTN.

3C.2 Electrical Field Dependence of Data Retention In High-k Interpoly Dielectrics, *Chun-Hyung Chung, Seung-Hyun Lim, Sang-Wook Lim, Young-Sun Kim, SY Choi, and Joo-Tae Moon*

Data retention characteristics of high-k interpoly dielectrics (IPD) with a fully planar stacked cell are investigated. We show that retention behavior simply depends on the electric field across the IPD, which is in quadratic inverse proportion to the IPD's reduced EOT. In order to overcome the scaling limits guaranteeing the memory cell's reliability, we propose a new high-k stack without the bottom oxide and achieve excellent reliability, less than 0.3V of charge loss with IPD EOT below 7nm. Based on a TAT model, we simulate the charge loss behavior through the high-k IPD.

3C.3 Characterization of Threshold Voltage Instability after Program in Charge Trap Flash Memory, *Bio Kim, SeungJae Baik, Sunjung Kim, Joon-Gon Lee, Bonyoung Koo, Siyoung Choi, and Joo-Tae Moon*

We investigated threshold voltage shifts after program pulse in charge trap flash memory by measuring drain current changes. We have found threshold voltage shifts can be characterized as a function of not only the materials of tunnel oxide, trap layer, blocking layer, but also physical parameters like device size and electrical measurement environment such as program voltage target and gate bias voltage. This approach can identify the root cause of initial threshold voltage shifts in charge trap flash memory devices.

3C.4 Study of Gate-Injection Operated Sonos-Type Devices using the Gate-Sensing and Channel-Sensing (GSCS) Method, *Pei-Ying Du, Hang-Ting Lue, Szu-Yu Wang, Tiao-Yuan Huang, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu*

SONOS devices using gate injection programming and erasing have better cycling endurance because the gate oxide is not stressed by P/E operations. This work studies the gate injection behavior in detail using the recently developed gate-sensing and channel-sensing (GSCS) technique. GSCS accurately locates the charge centroid during programming/erasing and reliability tests. For the first time, we can track the charge centroid for gate-injection "top BE-SONOS" and various SONOS-type devices. Our results indicate that the charge centroid after electron gate injection is close to the nitride center, irrespective of various nitride thickness and top dielectric. Moreover, there is electron and hole vertical mismatch after hole gate injection. Comparing the results from SONS, we can clearly prove that electrons are mainly distributed inside the bulk nitride instead of the interfaces between oxide and nitride. For SNOS and SNS, where there is electron and hole injection simultaneously, two-region approximation can give us more detailed information about electron and hole capture. By comparing experimental data with theoretical modeling, we have shown that nitride 7nm or thicker captures all the injected electrons up to total charge area density ~ $10^{13}cm^{-2}$.

3C.5 Study of Localized Tunnel Oxide Degradation after Hot Carrier Stressing Using A Novel Mid-Bandgap Voltage Characterization Method, *Cheng-Hung Tsai, Yen-Hao Shih, Yi-Hsuan Hsiao, Tzu-Hsuan Hsu, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu*

Hot carrier damage, especially by hot holes, limits the reliability performance of nonvolatile memories (NVMs). The damage creates localized traps in the tunnel oxide and localized interface traps at the oxide/silicon interface. In this paper, we propose a novel method to independently quantify trapped charges localized in the oxide and at the interface. We applied the new method to probe the oxide degradation in nitride trapping memory and found (i) the oxide traps (N_{OT}) capture both electrons and holes, (ii) the retention degradation involves interface trap (N_{IT}) annealing, electron de-trapping, and hole de-trapping, (iii) upon baking, N_{IT} annealing and electron de-trapping happen simultaneously while hole de-trapping dominates the long-term instability at 250°C, (iv) the V_T instability can be improved by using an interface strengthening nitridation process.

3C.6 Reliability of Single and Dual Layer Pt Nanocrystal Devices for NAND Flash Applications: A 2-Region Model for Endurance Defect Generation, *Pawan Singh, Gaurav Bisht, Siva Theja M, Sandhya C, Ralf Hofmann, Kaushal Singh, Gautam Mukhopadhyay, Nety Krishna, and Souvik Mahapatra*

Nanocrystal (NC) based memory devices are considered a possible alternative for floating gate (FG) replacement below 30nm node. In this work, endurance reliability of Pt NC devices is investigated for single layer (SL) and dual layer (DL) structures. The degradation in the devices due to Program/Erase (P/E) stress is investigated. Relative improvement in reliability of DL structure over SL structure is shown. A physical model for defect generation in the gate stack is proposed which is able to explain endurance and post-cycling characteristics. Dual layer structure is shown to have better inherent reliability over single layer structure.

3C.7 (Invited) Three Bits Per Cell Floating Gate NAND Flash Memory Technology for 30nm and Beyond, *Hiroyuki Nitta, T. Kamigaichi, F. Arai, T. Futatsuyama, M. Endo, N. Nishihara, T. Murata, H. Takekida, T. Izumi, K. Uchida, T. Maruyama, I. Kawabata, Y. Suyama, A. Sato, K. Ueno, H.Takeshita, Y. Joko, S. Watanabe, Y. Liu, H. Meguro, A. Kajita, Y. Ozawa, Y. Takeuchi, T. Hara, T. Watanabe, S. Sato, H. Tomiie, Y. Kanemaru, R. Shoji, C.H. Lai, M. Nakamichi, K. Owada, T. Ishigaki, G. Hemink, D. Dutta, Y. Dong, C. Chen, G. Liang, M. Higashitani, and J. Lutze*

Three bits per cell NAND Flash Memory Technology for 30nm and beyond has been successfully developed with floating gate technology. Tight natural Vth distribution, wide program/erase window, and good cell reliability such as program disturb, endurance and data retention are obtained. 8 level Vth distributions are successfully demonstrated.

Session 3E: Failure Analysis

Duluth/Mackenzie Rooms, 8:15 am
Chair: Ed Cole, Sandia National Laboratories

3E.1 Study of Formation Mechanism of Nickel Silicide Discontinuities in High Performance CMOS Devices, *Shuichi Kudo, Yukinori Hirose, Takuya Futase, Yoshifumi Ogawa, Tadashi Yamaguchi, Kotaro Kihara, Keiichiro Kashihara, Naofumi Murata, Toshiharu Katayama,Kyoichiro Asayama, and Eiichi Murakami*

We performed detailed analysis of Ni silicide discontinuities induced by agglomeration that causes the increasing electric resistance in high-performance CMOS devices by using advanced physical analysis techniques. We confirmed that the agglomeration of the Ni silicide is related to elongated-triangular-shaped-splits - which we call delta-shaped-splits - which cause discontinuities that occur at small-angle grain boundaries pinned by boron clusters even with small stress. We successfully determined the formation mechanism of the Ni silicide discontinuities in detail. It is essential to develop a highly reliable Ni salicide process, especially for 45 nm node high performance devices and beyond.

3E.2 (Invited) Material Analysis With a Helium Ion Microscope, *Larry Scipioni, William Thompson, Sybren Sijbrandij, and Shinichi Ogawa*

The helium ion microscope, a new imaging technology, is being applied also to sample modification. The application opportunity exists due to the extreme high resolution and the ability to gather analytical data as well as images. Possible applications include inspection, elemental analysis, and dopant concentration measurements.

3E.3 Methodology to Support Laser-Localized Soft Defects on Analog and Mixed-Mode Advanced ICs, *Magdalena Sienkiewicz, Abdellatif Firiti, Olivier Crepel, Philippe Perdu, Kevin Sanchez, and Dean Lewis*

The soft defect localization on analog or mixed-mode ICs is becoming more and more challenging due to their increasing complexity and integration. New techniques based on dynamic laser stimulation are promising for analog and mixed-mode ICs. Unfortunately, the considerable intrinsic sensitivity of this kind of devices under laser stimulation makes the defect localization results complex to analyze. As a matter of fact, the laser sensitivity mapping contains not only abnormal sensitive regions but also naturally sensitive ones. In order to overcome this issue by extracting the abnormal spots and therefore localize the defect, we propose in this paper a methodology that can improve the FA efficiency and accuracy. It consists on combining the mapping results with the electrical simulation of laser stimulation impact on the device. First, we will present the concept of the methodology. Then, we will show one case study on a mixed-mode IC illustrating the soft defect localization by using laser mapping technique & standard electrical simulations. Furthermore, we will argument the interest of a new methodology and we will show two simple examples from our experiments to validate it.

3E.4 Electron Beam Induced Temperature Oscillation For Qualitative Thermal Conductivity Analysis By An SThM / ESEM-Hybrid-System, *Anne Tiedemann, Ralf Heiderhoff, Ludwig Balk, and Jacob Phang*

A hybrid-system consisting of a Scanning Thermal Microscope and an Environmental Scanning Electron Microscope is used to analyze directional thermal conductivity mechanisms. An electron beam stimulates locally variable hot spots, whereas a thermal probe is used as a locally resolving detector. The detected temperature oscillation strongly depends both on the local thermal conductivity and on the directivity of the heat transport within the investigated sample. This may allow analysis of linear structures like interfaces within materials.

3E.5 Electron Beam Induced Current Investigation of Stress-Induced Leakage and Breakdown Processes in High-k Stacks, *Jun Chen, Takashi Sekiguchi, Naoki Fukata, Masami Takase, Toyohiro Chikyow, Ryu Hasunuma, Kikuo Yamabe, Motoyuki Sato, Yasuo Nara, and Keisaku Yamada*

We report dynamic and microscopic investigations of electrical stress induced defects in a high-k/metal gate stack by electron beam induced current (EBIC). The correlation between dielectric breakdown and EBIC sites are reported. A systematic study was performed on pre-existing and electrical stress induced defects. These defects are successfully visualized. The origin of pre-existing defects is discussed, comparing different gate electrodes and their temperature-dependence. These trap defects were successfully visualized by EBIC.

3E.6 Surface Electro-Static Discharge or Mechanical Damage: Solving the Mystery of Metal-to-Metal Shorts Using an Innovative Failure Analysis Approach, *Lesly Zaren Endrinal and Edward Coyne*

This paper introduces a new failure analysis procedure to distinguish Surface Electro-Static Discharge (ESD) from mechanically induced metal-to-metal shorts. The procedure utilizes two common techniques, Transmission Electron Microscopy (TEM) material analysis and Focused Ion Beam (FIB) cross sectioning. TEM analysis of the failure mechanism enables the material structure to be studied in order to distinguish the thermal from mechanical processes. Once a mechanical process has been confirmed, the formation of the failure mechanism is imaged through a new methodology for package analysis by means of backside cross-section using the Dual Beam FIB to show the molding compound interaction with the die surface for the first time.

Session 3F: Late Papers

Duluth/Mackenzie Rooms, 11:20 am

Chair: Hugh Barnaby, Arizona State University

3F.1 Adapted Strategies for Dew Condensation Testing to Evaluate the Reliability of Lead Free Surface Finishes, *Christian Matzner and K. Feldmann*

The advancing usage of electronic devices combined with the progressive trend of miniaturization and increasing functionalities, especially in automotive applications, sets high demands on reliability assurance. As complexity of systems and loads at mission location rise, suitable test strategies are needed, which provide expressive statements about products' reliability. In this article the influence of high humidity and dew condensation on current lead free surface finishes for electronic systems is examined under different climatic loads. Therefore special test patterns with the surface metallizations tin, silver, nickel/gold and Organic Solderability Preservative (OSP) were stressed with a static and two cyclic temperature-humidity test profiles. Both fault times of the different materials and efficiency of the applied test were evaluated with different criteria. In order to investigate fault times, failure mechanisms and evaluation criteria a high precise measurement chain was conceived, to continuously monitor the designed specimens while testing. During the tests both static and sporadic failures with and without optical evidence could be revealed. Depending on climatic profile and used evaluation criterion, the failure times and number of occurred failures varied. According to climatic load and inspected line/space width, the considered materials showed great differences in reliability.

WEDNESDAY AFTERNOON
April 29, 2009

Session 4A: Process and Integration

Le Grand Salon, 2:10 pm

Chair: Koji Eriguchi, Kyoto University

4A.1 (Invited) Reliability for Manufacturing on 45nm Logic Technology With High-k + Metal Gate Transistors and Pb-free Packaging, *Rahim Kasim, Chris Connor, Jeff Hicks, Jason Jopling, and Chris Litteken*

This paper addresses several key aspects of integrated reliability for the Intel 45nm logic technology with high-K metal gate (HK+MG) transistors and Pb-free packaging. Significant changes in process architecture and materials were introduced and careful integration and manufacturing innovations were needed to meet historical expectations for transistor, defect, and package reliability. Furthermore the stability of intrinsic and defect reliability performance needed to be demonstrated. Highly accelerated TDDB and bias temperature instability (BTI) tests were implemented to enable very high sampling rates, establishing stable transistor reliability in high manufacturing volumes. Integrated product defect reliability results are presented showing that the historical correlation to yield defect density for stable manufacturing processes is maintained on this generation into an even lower fail rate regime. Similarly, volume package reliability monitor data are shown validating thermo-mechanical stability of the 1st level Pb-free package interconnect.

4A.2 Impact of Metal Gate Electrode on Weibull Distribution of TDDB in HfSiON Gate Dielectrics, *Izumi Hirano, Yasushi Nakasaki, Shigeto Fukatsu,Akiko Masada, Yuichiro Mitani, Koji Nagatomo, Masakazu Goto, Seiji Inumiya, and Katsuyuki Sekine*

The slope parameter of Weibull plot of Tbd, β, strongly depends on gate electrode material for metal-gate/HfSiON gate stacks in n-FETs. Furthermore β of Tbd under bipolar stress is larger than that under DC stress. From these results, it is found that the balance of injected carriers is strongly related to β in terms of the origin of large β for metal-gate/high-k.

4A.3 Detrimental Impact of Technological Processes on BTI Reliability of Advanced High-k/Metal Gate Stacks, *Xavier Garros, Mikael Casse, Claire Fenouillet-Béranger, Gilles Reimbold, Francois Martin, Clément Gaumer, Claudia Wiemer, M. Perego, and Fabien Boulanger*

A systematic study of mobility performances and Bias Temperature Instability (BTI) reliability was done on a large variety of advanced dielectric stacks. We clearly demonstrate that mobility performances and NBTI reliability are strongly correlated and

that they are affected by the diffusion of nitrogen species N at the Si interface. Reducing the metal gate thickness favors the reduction of mobility degradations and NBTI, but, also strongly enhances PBTI, due to a complex set of reactions in the gate oxide. An optimum gate thickness must be found to obtain an acceptable trade off between device performance and reliability requirements.

4A.4 Dual Nature of Metal Gate Electrode Effects on BTI and Dielectric Breakdown in TaC/HfSiON MISFETs, *Shigeto Fukatsu, Izumi Hirano, Kosuke Tatsumura, Akiko Masada, Shosuke Fujii, Yuichiro Mitani, Masakazu Goto, Seiji Inumiya, Kazuaki Nakajima, Shigeru Kawanaka, and Tomonori Aoyama*

We investigated bias temperature instability (BTI) and time dependent dielectric breakdown (TDDB) in TaCx/HfSiON MOSFETs in terms of the effects of TaCx metal gate electrode, using various Ta composition and TaCx thickness. We find a dual nature of TaCx metal gate electrode effects on the reliability. The gate electrode has both positive and negative influence on BTI and TDDB. Though various TaCx layers were deposited on the same HfSiON layer, high composition of Ta in the TaCx layer and thick TaCx layer improve BTI and mobility, while they deteriorate time to breakdown (Tbd) because of the effect of metal gate induced defects.

4A.5 Processing Impact on the Reliability of Single Metal Dual Dielectric (SMDD) Gate Stacks, *Thomas Kauerauf, Marc Aoulaiche, Moon Ju Cho, Lars-Ake Ragnarsson, Tom Schram, Robin Degraeve, Thomas Hoffmann, Guido Groeseneken, and Serge Biesemans*

The impact on the reliability of cap layers for low V_t nMOS and pMOS high-k transistors with metal gate is investigated and devices without the resist and strip process are compared to different resist removal recipes. It is found that the interface is not affected by the cap layer, but during the resist removal a thin defect layer is created. While with the capping above the host dielectric the impact of this defect layer is minor, with the capping located below the host the defects are more efficient, increasing the leakage current and reducing the TDDB lifetime.

4A.6 Degradation of Interface Integrity Between a High-k Dielectric Thin Film and a Gate Electrode Due To Excess Oxygen in the Film, *Hideo Miura, Ken Suzuki, Yuta Ito, Seiji Samukawa, Tomonori Kubota, Toru Ikonma, Hideki Yoshikawa, Shigenori Ueda, Yoshiyuki Yamashita, and Keisuke Kobayashi*

In this study, the degradation mechanism of the interface integrity between a hafnium dioxide thin film and a gate electrode thin film was investigated by using quantum chemical molecular dynamics. Effect of point defects such as excessive oxygen and carbon interstitials in the hafnium dioxide films on the formation of the interfacial layer between them was analyzed quantitatively. Though the defect-induced sites caused by oxygen vacancies and carbon interstitials were recovered by additional oxidation after the deposition of the hafnium oxide film, the excessive interstitial oxygen and carbon atoms remained in the film deteriorated the quality of the interface by forming new oxide or carbide of the deposited metal such as tungsten and aluminum. No interfacial layer was observed when a gold thin film was deposited on the hafnium oxide. The estimated changes of the interface structure were confirmed by experiments using synchrotron radiation photoemission spectroscopy. [*Keywords:* High-k Gate Dielectrics, Band Gap, Point Defects, Residual Stress, Hafnium Oxide, Quantum Chemical Molecular Dynamics, Synchrotron-radiation Photoemission Spectroscopy]

Session 4B: Nanoelectronics

Marquette/Jolliet Rooms, 2:10 pm
Chair: Jeff Peterson, Intel and Vice Chair: Curt Richter, NIST

4B.1 Random Telegraph Noise in Highly Scaled nMOSFETs, *Jason Campbell, Jin Qin, Kin Cheung, Liangchun Yu, John Suehle, Anthony Oates, and Kuang Sheng*

Recently, 1/f and random telegraph noise (RTN) studies have used a noise framework which involves charge exchange between the inversion layer and the bulk dielectric defects via elastic tunneling to infer information about bulk dielectric defects' spatial and energetic distributions. In this study, we extracted the characteristic capture and emission time constants from RTN in highly scaled nMOSFETs and showed that they are inconsistent with the elastic tunneling picture dictated by the physical

thickness of the gate dielectric. These results suggest that a large body of the recent RTN and 1/f noise defect profiling literature very likely needs re-interpretation.

4B.2 V_{TH} Fluctuations Due to Random Telegraph Signal on Work Function Control in Hf-Doped Silicate Gate Stack, *Tatsuo Shimizu, Ichiro Kato, Shinji Yokogawa, Takashi Kitagaki, Jun Taniguchi, Takatomo Suzuki, and Takashi Tsuboi*

We investigated *V*th fluctuations due to random telegraph signal (RTS) on gate work function control in Hfdoped silicate gate stack compared with the conventional impurity doping. Complex RTS were recognized for both n- and p-MOSFET. The WFC does not appreciably affect *V*th fluctuations for n-and p-MOSFET. However, dopant contributes to *V*th fluctuation, especially for the p-MOSFET. We found it is caused by change in *V*fb fluctuation due to increase of the trap density.

4B.3 Cu-ion Diffusivity in SiO_2-Ta_2O_5 Solid Electrolyte and Its Impact on The Yield of Resistance Switching After BEOL Processes, *Naoki Banno, Toshitsugu Sakamoto, Hiromitsu Hada, Naoki Kasai, Noriyuki Iguchi, H. Imai, Shinji Fujieda, Toshinari Ichihashi, Tsuyoshi Hasegawa, and Masakazu Aono*

For stability against the thermal budget of the CMOS BEOL process, we developed a new solid-electrolyte switch that uses a SiO_2-Ta_2O_5 composite as the electrolyte. This switch has high thermal stability because thermal diffusion of Cu^+ ions is suppressed in the composite. Moreover, its switching characteristics after thermal annealing are similar to those of a Ta_2O_5 switch without annealing. The switch with the SiO_2-Ta_2O_5 composite electrolyte has good ON-state durability against DC current stress; its durability is comparable to that of a single via in interconnects. The switch can be implemented in the local interconnection layers of LSIs.

4B.4 Investigation on Hot Carrier Reliability of Gate-All-Around Twin Si Nanowire Field Effect Transistor, *Yun Young Yeoh, Sung Dae Suk, Ming Li, Kyoung Hwan Yeo, Dong-Won Kim, Gyoyoung Jin and Kyoungsuk Oh*

Hot carrier (HC) reliability of Gate-All-Around Twin Si Nanowire Field Effect Transistor (GAA TSNWFET) is reported and discussed with respect to size and shape of nanowire channel, gate length, thickness and kind of gate dielectric in detail. Smaller nanowire channel size, shorter gate length and thinner gate oxide down to 2nm thickness show worse hot carrier reliability. The worst V_D for 10 years guaranty, 1.31V, satisfies requirement of ITRS roadmap.

4B.5 (Invited) Avalanche, Joule Breakdown and Hysteresis in Carbon Nanotube Transistors, *Eric Pop, Sumit Dutta, David Estrada, and Albert Liao*

We explore several aspects of reliability in carbon nanotube transistors, including their physical dependence on diameter. Avalanche behavior is found at high fields (5-10 V/μm), while Joule breakdown is reached at high current and heating, in the presence of oxygen. Finally, we describe a method for minimizing hysteresis effects via pulsed measurements. *Session 4C: High Voltage.*

Session 4C: High Voltage

Duluth/Mackenzie Rooms, 2:10 pm
Chair: Peter Moens, AMI Semiconductors

4C.1 (Invited) Reliability Challenges for Power Devices under Active Cycling, *Werner Kanert*

Power stages are subject to severe stress due to active cycling, resulting in e.g. fast thermal cycling. Requirements for, e.g., motor management in automotive applications comprise up to several hundred millions of cycles under normal operation conditions and additional “disturbances” such as load dump and short circuit events with high energy pulses. Such pulses lead to high power dissipation in the device, leading to an inhomogeneous and time-dependent temperature distribution in the device. Severe metal degradation can be caused by this stress, resulting in a final catastrophic failure of the device. This issue is neither addressed by “classical” reliability methods applied to silicon wafer technology nor by standard product qualification procedures. Robustness Validation applies the principles of failure-mechanism-driven reliability to qualification of semiconductor devices for automotive applications. Based on these principles, a characterization strategy is defined that

contains derivation of corresponding design rules from accelerated test structure reliability data and combines these design rules with product requirements in the product development process. 3D electro-thermal simulation is an indispensable ingredient of this strategy that is needed for conversion of application conditions (e.g. inductance of load) to technology relevant data (e.g. temperature increase due to voltage/current pulse). Using this strategy, data can be generated that can be referenced in further product development projects. The proposed methodology is essential for designing in reliability into the product.

4C.2 Hot Carrier Effects in Trench-Based Integrated Power Transistors, *Peter Moens, Jaume Roig, Bart Desoete, Filip Bauwens, and Marnix Tack*

This paper reports for the first time on anomalous hot carrier effects observed in vertically integrated trench-based (TB-MOS) power transistors. The avalanche current reaches a maximum at intermediate drain voltage, and decreases for increasing drain voltage. The hot carrier lifetime of the transistors yields a minimum at intermediate drain voltage, and not at the maximum drain voltage. Charge pumping experiments enable to locate the degradation in the TB-MOS. A degradation model is proposed.

4C.3 A New Off-State Drain-Bias TDDB Lifetime Model for DENMOS Device, *Shu Wen Chang, Chia Lin Chen, C.J. Wang, and Kenneth Wu*

For the first time, a new off-state drain-bias TDDB lifetime model is proposed for DENMOS devices. With the new model, the off-state drain-bias TDDB lifetime can be well predicted from the conventional gate-bias stress without extra long term drain-bias stress. The TDDB lifetime can be decoupled to three components; the small effective stress area and large voltage drop shared by the drain-extension region increase the lifetime, and the band-to-band tunneling current degrades it. The mechanism of oxide breakdown with the off-state drain-bias is also well understood as the oxide traps distributed from the center of channel to the drain side.

4C.4 Hot Carrier Stress Degradation Modes in p-type High Voltage LDMOS Transistors, *Hubert Enichlmair, Jong-Mun Park, Sara Carniello, Bernhard Loeffler, Rainer Minixhofer, and Max Levy*

The hot carrier stress induced device degradation of a p-type LDMOS high voltage transistor is investigated at different stress conditions. The influence of shallow trench corner rounding and carbon ion implantation into the shallow trench region is discussed. Numerical device simulations, charge pumping measurements and electrical characterisations are used for these investigations.

4C.5 TDDB Evaluations and Modeling of Very High-Voltage (10KV) Capacitors, *Robert Higgins and Joe McPherson*

Time-Dependent Dielectric Breakdown (TDDB) data for very thick (8um) silica-based dielectrics is reported at relatively low fields (< 5MV/cm) but at extremely high voltages (up to 4000V). TDDB data was taken across a wide range of dielectric thicknesses ranging from 38Å to 8µm (80,000Å). Consistent with the TDDB results generally reported for thin films, a thickness-independent effective dipole moment of ~13eÅ was concluded from the testing data. TDDB data is also presented for stacked dielectrics structures (Nitride/ Silica) which tend to show a strong polarity dependence, depending on whether electron injection is into the nitride or oxide layer. While the time to failure is polarity dependent, the effective dipole moment is independent of polarity.

4C.6 Improvement of the Electrical Safe Operating Area of a DMOS Transistor during ESD Events, *Alevtina Podgaynaya, Dionyz Pogany, Erich Gornik, and Matthias Stecher*

Electrical safe operating area (SOA) of double-diffused vertical MOSFETs (VDMOS) in smart power ICs is investigated by simulation and experiments. The influence of the layout of VDMOS cells is analyzed. DMOS transistors with circular/oval cell layout exhibit higher ESD robustness in comparison with conventional stripe cells. The effect is related to better current distribution of circular/oval cell devices. It is also observed that appropriate source/body engineering can improve electrical SOA of a VDMOS as well.

Reception and Poster Presentations
Wednesday, April 29, 7:00 pm – 9:00 pm, Hochelaga Room

AP - Assembly and Packaging Posters

AP.1 Performance and Reliability Analysis of 3D-Integration Structures Employing Through Silicon Via (TSV), *Aditya Karmarkar, Xiaopeng Xu, and Victor Moroz*

Large thermal mismatch stress can be introduced in 3D-Integration structures employing Through-Silicon-Via (TSV). The stress distribution in silicon and interconnect is affected by the via diameter and layout geometry. The TSV induced stress changes silicon mobility and ultimately alters device performance. The mobility and performance change differs in nand p-silicon and is a function of the distance to the TSV. In addition, the TSV induced stress acts on the barrier layer, the landing pad, the interconnects, and the dielectrics. The interactions with defects may lead to crack nucleation and growth, and compromise the structure reliability. Furthermore, the material choice that reduces silicon stress for less impact on performance may increase stresses in other regions where reliability is of concern. This paper studies these effects and their dependence on various integration configurations.

BD - Device Dielectric Breakdown Posters

BD.1 Soft Breakdown in MgO Dielectric Layers, *Enrique Miranda, Eamon O'Connor, Greg Hughes, Patrick Casey, Karim Cherkaoui, Scott Monaghan, Rathnait Long, Dan O'Connell, and P.K. Hurley*

In this work, we report on the occurrence of the soft breakdown (SBD) failure mode in 20nm-thick films of magnesium oxide (MgO) grown on Si substrates. To our knowledge, this is the first observation of this failure mechanism in a high-κ gate dielectric with such a large oxide thickness. We show that the I-V characteristics follow the power-law dependence typical of SBD conduction in a wider voltage range than that reported for SiO_2. We pay special attention to the relationship between the magnitude of the current and the normalized differential conductance, and analyze the role played by the injection polarity and substrate type.

BD.2 Probing the Electronic Structure of Defective Oxide: an EELS Approach, *Xiang Li, Gang Zhang, Chih Hang Tung, and Kin Leong Pey*

Combining monochromatic scanning transmission electron microscopy (M-STEM) with electron energy loss spectroscopy (EELS), the electronic structures of the defective oxide after breakdown (BD) have been studied. Our results show that the electronic structures of the defective oxides are similar to the oxygen deficient substoichiometric-oxide. The SiO_2 bulk properties are lost along with oxygen vacancy formations in the breakdown oxide.

BD.3 Critical Gate Voltage and Digital Breakdown: Extending Post-Breakdown Reliability Margin in Ultrathin Gate Dielectric with Thickness < 1.6 nm, *V. L. Lo, K. L. Pey, R. Ranjan, C. H. Tung, J. R. Shih, and Kenneth Wu*

The saturation of a critical gate voltage at 2-2.4 V for SiON with thickness < 1.6 nm (EOT < 1.4 nm) extends the role of digital breakdown (BD) in prolonging progressive BD at nominal voltages. As a result, the post-BD gate leakage degradation rate, which is extrapolated from a high voltage using the conventional approach, is highly overestimated, warranting one to revise the post-BD reliability assessment.

BD.4 A New Detection Method of Soft Breakdown in Ultra-Thin Gate Oxides by Light-Emission Analysis, *Kohji Ohgata, Makoto Ogasawara, Masami Kawakami, Tohru Koyama, and Eiichi Murakami*

We attempted the new breakdown detection method instead of V-RAMP test, and clarified that the localized SBD in ultra-thin oxides with the large direct tunneling current in which masks the SBD event can be detected by using the adequate threshold of the intensity in light-emission analysis by inverted emission microscope with InGaAs camera. In addition, we confirmed that the defect density calculated from light-emission analysis of Tr. Array TEG approximately corresponds to the product failures caused by the SBD of gate oxides. This new detection method can be a WLR tool for monitoring oxides integrity.

BD.5 Real-Time Observation of Trap Generation by Scanning Tunneling Microscopy and the Correlation to High-k Gate Stack Breakdown, *Yi Ong, Diing Ang, Kin Pey, Sean O'Shea, Kuniyuki Kakushima, Takamasa Kawanago, Hiroshi Iwai, and Chih-Hang Tung*

Due to an inherently high concentration of non-equilibrium defects in the Hκ gate stack [2], interpretation of the statistics of conventional methodology (e.g. TDDB) based on established understanding of the SiO_2/SiON system leads to unrealistic outcomes [1]. Using Scanning Tunneling Microscopy (STM), we demonstrate the capability in spatially mapping electronic traps in respectively layers of high-κ gate stack of the next generation. We manage to study the evolution of trap generation in the Hκ and SiO_x interfacial layer (IL) within a "trap-free" area of the Hκ gate stack [3]. In this work, we look into the role of localized electronic traps in the evolution of trap generation in the Hκ and IL by inducing electrical stress locally on the individual traps. By monitoring trap generation in the respective layers of the Hκ gate stack, we propose a model describing how soft breakdown (SBD) can be triggered by pre-existing or electrically induced electronic traps.

BD.6 Comprehensive Physics-Based Breakdown Model for Reliability Assessment of Oxides with Thickness Ranging from 1nm to 12nm, *Ernest Wu, Jordi Sune, and Rolf-Peter Vollertsen*

The state-of-art understanding on the T_{BD} voltage acceleration models in direct tunneling (DT) and Fowler-Nordheim (FN) regimes is thoroughly and carefully reviewed including recent work on thin oxides as well as historical publication database for thick oxides. The field-driven T_{BD} exponential law is found to be inconsistent with many experimental findings. We present a comprehensive physics-based breakdown model, which separately takes the roles of tunneling current and defect generation efficiency into account, and it is consistent with many experimental findings for thickness from 1.0nm to 12nm. With these new advanced understandings, we can now resolve many controversies surrounding T_{BD} voltage acceleration models for SiO_2-based dielectrics. Finally, a practical solution of acceleration model for TDDB qualification is proposed.

CD - Compound Semiconductors Posters

CD.1 Strain Induced Buffer Layer Defects In GaN HFETs and Their Evolution during Reliability Testing, *Yinsin Li, M. Krishnan, Shahrzad Salemi, Gary Paradee, and Aris Christou*

The reliability physics of GaN HFETs has been investigated in order to identify strain related traps originating at the GaN/SiC substrate interface. The buffer layers investigated were deposited by MBE techniques at a series of growth temperatures and thicknesses so as to attain buffer layers with variable trap density. Heterojunction transistors (HFETs) based on AlGaN/GaN heterostructures have been modeled and the results are described in this paper.

CD.2 Physical Mechanism of Buffer-Related Lag and Current Collapse in GaN-Based FETs and their Reduction by Introducing a Field Plate, *Atsushi Nakajima, Keiichi Itagaki, and Kazushige Horio*

Two-dimensional transient analysis of field-plate AlGaN/GaN HEMTs and GaN MESFETs is performed, considering a deep donor and a deep acceptor in the semi-insulating GaN buffer layer. Quasi-pulsed *I-V* curves are derived from the transient characteristics. It is studied how the existence of a field plate affects buffer-related drain lag, gate lag and current collapse. It is shown that in both FETs, the drain lag is reduced by introducing a field plate, because electron injection into the buffer layer is weakened by it, and trapping effects are reduced. The dependence on SiN passivation layer thickness under the field plate is also studied, suggesting that there is an optimum thickness of the SiN layer to minimize buffer-related current collapse and drain lag in GaN HEMTs and MESFETs.

CD.3 Analysis of Degradation Induced by Silicon Nitride in InP/InGaAs Heterojunction Bipolar Transistors, *Dan Sachelarie*

The Si_3N_4 layer deposited by PECVD at 300°C to passivate InP/InGaAs HBTs induces extra charges densities in the peripheral mesa emitter-base heterojunction. The changes in the effective emitter-base doping concentrations were determined by a new

method which used the simultaneous analysis of the collector current density and the collector current ideality factor, measured at a fixed emitter-base voltage.

CD.4 False Surface-Trap Signatures Induced by Buffer Traps in AlGaN-GaN HEMTs, *Giovanni Verzellesi, Mustapha Faqir, Alessandro Chini, Fausto Fantini, Gaudenzio Meneghesso, Enrico Zanoni, Francesca Danesin, Franco Zanon, Fabiana Rampazzo, Fabio Marino, Anna Cavallini, and Antonio Castaldini*

Buffer traps can induce "false" surface-trap signatures in AlGaN-GaN HEMTs, namely the same type of current-mode DLTS peaks and pulse responses that are generally attributed to surface traps. Device simulations are adopted to clarify the underlying physics. Being aware of the above phenomenon is important for both reliability testing and device optimization, as it can lead to erroneous identification of the degradation mechanism, thus resulting in inappropriate correction actions on the technological process.

CD.5 Analysis of Diffusion Involved in Degradation of InGaN-Based Laser Diodes, *Kenji Orita, Shinichi Takigawa, Masaaki Yuri, Tsuyoshi Tanaka, Matteo Meneghini, Nicola Trivellin, Lorenzo Trevisanello, Enrico Zanoni, and Gaudenzio Meneghesso*

The gradual increase of threshold current in InGaN-based blue laser diodes (LDs) submitted to stress tests is generally attributed to the increased density of non-radiative recombination centers (NRCs) which is induced by diffusion. However, this hypothesis has not been verified yet. In this paper, we analyze the variation in non-radiative recombination lifetime of InGaN LDs during ageing to extract the value of the diffusion coefficient that is related to degradation. The obtained results support that the increased density of NRCs is related to dislocation-mediated diffusion. The demonstrated method constitutes a powerful tool for the study of degradation in LDs.

CR - Circuit Reliability Posters

CR.1 Failure Mechanisms in CMOS-based RF Switches Subjected to RF Stress, *Anuj Madan, Tushar Thrivikraman, and John Cressler*

We investigate the reliability of RF switches for high-power, high dynamic range RF applications. Switches in two different CMOS technology platforms (180 nm and 130 nm) were observed to fail catastrophically beyond 33 dBm RF input power. The switches were single-pole double-throw with series-shunt topology. The reliability of a standalone switching series transistor from a single-pole double-throw switch was analyzed to investigate the failure mechanisms involved. Gate dielectric breakdown at high RF input power is demonstrated to lead to the failure of RF switches. Finally, the effect of transistor failure on switch operation is discussed.

CR.2 Impact of NBTI and PBTI in SRAM Bit-cells: Relative Sensitivities and Guidelines for Application-Specific Target Stability/Performance, *Aditya Bansal, Rahul Rao, Jae-Joon Kim, Sufi Zafar, James Stathis, and Ching-Te Chuang*

The stability and performance characteristics of Static Random Access Memories (SRAMs) are known to degrade with time due to the impact of Negative and Positive Bias Temperature Instabilities (NBTI (in PFET) and PBTI (in NFET)). In this work, we provide insights into *relative sensitivities* of these phenomena on speed and stability of SRAM cells. Relative impact on access time, stability, and tolerability of one phenomenon over another has been studied for different application specific (high-performance or low-power) SRAM cells. We show that high-performance SRAM cells should have lower VT drift due to PBTI compared with dense cells to contain READ stability and access time. Further, worst-case static stress poses tighter process constraints compared with alternating stress.

EL - ESD and Latchup Posters

EL.1 Ultra-Low-Leakage Power-Rail ESD Clamp Circuit in Nanoscale Low-Voltage CMOS Process, *Po-Yen Chiu, Ming-Dou Ker, Fu-Yi Tsai, and Yeong-Jar Chang*

A new power-rail ESD clamp circuit with ultra-low-leakage design is presented and verified in a 65-nm CMOS process with a leakage current of only 116nA at 25°C, which is much smaller than that (613µA) of traditional design. Moreover, it can achieve ESD robustness of over 8kV in HBM and 800V in MM ESD tests, respectively.

EL.2 Highly Resistive Body STI NDEMOS: An Optimized DEMOS Device to Achieve Moving Current Filaments for Robust ESD Protection, *Mayank Shrivastava, Jens Schneider, Maryam Baghini , Harald Gossner, and V. Ramgopal Rao*

A novel DeMOS device with modified body and source region in grounded gate (gg) NMOS configuration for ESD protection is proposed. Detailed 3D simulations indicate a high failure threshold because of moving current filaments and self-protection from gate oxide breakdown, even for fast transients. A detailed physics of second basepushout and moving filaments is discussed.

EL.3 Latchup Test Failure From ESD Protection Circuit Activation Beyond ESD Stress Condition, *I-Cheng Lin, Che-Yuan Jao, Rei-Fu Huang, Cheng-Hsing Chien, Chien-Hui Chuang, Chen-Feng Chiang, and Bo-Shih Huang*

Latchup test failures occurred at two IO pins of an IC. Failure analysis revealed damage at the ESD device of a neighboring power pins ESD protection circuit. To identify the cause of the problem, the behavior of the ESD circuit in response to the latchup trigger signal was monitored. The ESD protection circuit was found to anomalously respond to even DC-like latchup trigger pulses. Layout and circuit study identified a possible rare failure mode and subsequent experiments validated the suspected failure mechanism. A simple circuit modification successfully solved the issue without affecting discharge characteristic and ESD performance of the IC.

Heterostructure Laser Diodes, *Hiroyuki Ichikawa, Shinji Matsukawa, Kotaro Hamada, Akira Yamaguchi, and Takashi Nakabayashi*

We clarified the mechanism of forward-biased electrostatic-discharge-induced degradation of InP-based laser diodes. This degradation was caused by melting of the active layer as a result of light absorption. We observed a reduction in tolerance on aging in uncoated laser diodes. This reduction was suppressed by facet coating.

EL.5 Very Fast Transient Simulation and Measurement Methodology For ESD Technology Development, *Slavica Malobabic, David Ellis, Juin Liou, Javier Salcedo, Jean-Jacques Hajjar, and Yuanzhong Zhou*

A Transient safe operating area (TSOA) definition for ESD applications is introduced. Within this concept framework, ESD protection device topologies developed in a mixed-signal submicron high-voltage CMOS technology are studied to identify turn-on voltage and the resulting voltage overshoot conditions during fast ESD transients. A state-of-the-art numerical simulation environment used to study and optimize the fast transient response of ESD protection devices is discussed and simulation results are benchmarked versus very fast transmission line pulsing measurements. Constraints for triggering control of clamp devices are also investigated via simulations and pulse measurements.

EL.6 Characterization of the Electrostatic Discharge Induced Interface Traps in Metal-Oxide-Semiconductor Field-Effect Transistors, *Jen-Chou Tseng and Jenn-Gwo Hwu*

The interface trap's characteristics in silicon dioxide induced by electrostatic discharge current impulse were studied using the transmission line pulsing technique and charge pumping method. It was observed that the electrostatic discharge stress induces far less amount of interface traps prior to breakdown and the interface traps distribution along the channel direction is more non-uniform and localized than dc stress. The possible mechanisms for interface trap generation and formation are suggested. [*Keywords:* ESD, interface traps, oxide integrity, semiconductor reliability.

EX - Extreme Environments Posters

EX.1 Why is Oxide-Trap Charge-Pumping (OTCP) Method Appropriate for Extracting the Radiation-Induced Traps in MOSFET?, *Boualem Djezzar, Hakim Tahi, and Arezki Mokrani*

Oxide-trap charge-pumping (OTCP) method is used to estimate radiation-induced oxide-, interface-, and border-traps in complementary N-A and P-MOS transistors. We conduct a critical comparison between OTCP and classical methods like subthreshold slope (STS), Mid gap (MG), dual-transistor charge-pumping (DTCP), and dual-transistor border-trap (DTBT). On the one hand, OTCP offers more accurate densities of radiation-induced interface-traps (ΔN_{IT}) and border-traps (ΔN_{BT}), while STS and MG overestsimate ΔN_{IT} because both interface – and border-trap are sensed like interface-traps. On the other hand, OTCP estimates ΔN_{IT}, ΔN_{BT}, and radiation-induced oxide-trapped positive charge (ΔN_{OT}) for N- and P-Mos separately, whereas DTCP and DTBT give average densities for both devices.

EX.2 Laser Measurement Techniques For Detecting Age-Related Degradation of Device Radiation Response, *Kevin Horn*

The potential for aging effects in silicon electronics is a concern for systems with prolonged service lives that contain electronics that must function in extreme radiation environments. A set of laser-based diagnostic techniques is described that is used to provide on-going awareness of changes in the radiation resonse of aging discrete and integrated circuits. /This work was supported by the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration.

EX.3 Analysis of Radiation-Hardening Techniques for 6T SRAMs with Structured Layouts, *Gabriel Torrens, Bartomeu Alorda, Sebastià Bota, and Jaume Segura*

We analyze two complementary radiation-hardening techniques for 6T SRAMs compatible with structured layouts. One approach relies on selecting the Vt of each of the four transistors forming the SRAM cell inverters. The other one involves the modification of the widths of all pmos and nmos transistors of the cell. The first technique does not affect the cell layout. The second one increases the minimum width of all pmos by a factor Cp and the minimum width of all nmos by a factor Cn. This prevents the formation of diffusion bends, allowing structured layouts. Both techniques improve SEU robustness.

FA - Failure Analysis Posters

FA.1 Determination of the Electric Field Distribution within Multi-Quantum-Well Light Emitting Diodes by the use of Electron Beam Induced Methods, *Thomas Geinzer, Ralf Heiderhoff, and Ludwig Josef Balk*

Dynamic electron beam induced methods are applied to determine the local electrical field distribution of devices with small depletion regions. The dissipation volume generated by the electron beam is much larger than the depletion region during these investigations. The frequency behavior of the electron beam induced signal must be analyzed in order to determine the field strength accurately. Additionally, change of the collection efficiency due to the depletion region widening effect at different biasing conditions has to be taken into account. The advantage and possibility of this technique are demonstrated exemplarily for a commercial multi-quantum-well light emitting diode.

FA.2 A Study of Bipolar Phototransistor Action Existing in CMOS Process Triggered By a Laser Beam used in a C-AFM System, *Hung-Sung Lin, Mong-Shen Wu, and Tsui-Hua Huang*

A beam bounce technique in a conductive atomic force microscope (C-AFM) system is usually used to enable the probe head to measure extremely small movements of the cantilever as it is moved across the surface of the sample. However, the laser beam used for the beam bounce also gives rise to the photoelectric effect while we are measuring electrical characteristics of a device. The photoelectric effect occurring in NMOSFETs caused by a laser beam used in the C-AFM system has been reported [1]. In

this study, the photoelectric effect occurring in PMOSFETs will be discussed. An example that an invisible implant defect in a PMOSFET was successfully identified using the C-AFM based on the measured electrical characteristics and the bipolar phototransistor action models will also be introduced.

FA.3 Reliable and Accurate Temperature Measurement using Scanning Thermal Microscopy with Double Lock-In Amplification, *H.W. Ho, X.H. Zheng, J.C.H. Phang, and L.J. Balk*

Resistive-based scanning thermal microscopy (SThM) determines local temperature by establishing contact between probe and sample-under-test (DUT). Accurate temperature measurement is dependent on probe-DUT contact area which varies with DUT topography and probe geometry. Stability of the system to background temperature drift and electronic noise also affects accurate temperature measurement. A SThM technique incorporating double lock-in amplification is developed to overcome these limitations. The localized temperature change of an interconnect biased with a switching current supply is measured with improved signal level and a significant reduction of topographic influences. This allows for any heat source to be accurately localized.

FA.4 Unique Electrical Characterization and In-Line Monitoring of Nano-Tipped Defects in Metal-Insulator-Metal Capacitors, *Lieyi Sheng, Eric Snyder, Jason Doub, Valerie Berti, Levi Kriner, and Eddie Glines*

The unique characteristics of defective MIM capacitors under nano-ampere current injection and passive voltage contrast have verified the field enhancement and charge accumulation along nano-tipped defects. An improved process which reduces the risk of nano-whiskers is confirmed by in-line optical monitoring in production.

FF - Fabless and Foundry Posters

FF.1 Addressing IC Component Quality and Reliability Assurance Challenges, *Shi-Jie Wen, Rao Morusupalli, and Marc Hartranft*

This paper highlights some of the key challenges for the Quality and Reliability of semiconductor components based on field return data and root cause Pareto analysis. Some key learnings are discussed. The paper also discusses the topic of the role of organizations, its tasks and infrastructure necessary to achieve the required IC component quality and reliability. Specific examples are discussed. In the second part of this paper we discuss and summarize some of the reliability challenges experienced from the perspective of a customer for fabless semiconductor companies.

IC - Interconnect and BEOL Dielectrics Posters

IC.1 Withdrawn

IC.2 TDDB Lifetime of Asymmetric Patterns and Its Comprehension from Percolation Theory, *Hiroshi Miyazaki and Daisuke Kodama*

TDDB-lifetime distribution of asymmetric pattern was estimated using a 3-dimensional electrostatic model calculation and its statistical treatment based on the percolation theory. Nanometer-size small cells which represent the minimum unit of electric isolation are placed along the perimeter of an asymmetric pattern. A dielectric breakdown occurs when a series of defective cells form a path through the potential barrier. The local electric field near the cathode dictates the percolation-path length. This model suggests that a negative bias at the pattern tips provides a shorter percolation path due to steep gradient of potential, resulting in a shorter lifetime.

IC.3 Statistical Outlook into the Physics of Failure for Copper Low-k Intra-Metal Dielectric Breakdown, *Nagarajan Raghavan and Krishnamachar Prasad*

The degradation of low-k dielectrics is analyzed from a trap-assisted tunneling (TAT) current perspective assuming a Poole-Frenkel (P-F) conduction mechanism. A robust probabilistic failure model is developed which accounts for the development of

traps at the low-k - SiN capping layer interface which is believed to be the weak link for evolution of low-k dielectric failure mechanisms. The developed model also accounts for the bond breaking phenomenon as dangling bonds are suggested to be the functional form of trap centers during the evolution of the percolation path. The new model is observed to provide an accurate fit to the failure data in the literature. The statistical nature of time-dependent dielectric breakdown (TDDB) failure is shown to be dependent on the definition of failure and based on the conventional definition of catastrophic leakage current increase, we show that the Lognormal distribution is inapplicable and that the Weibull stochastics needs to be used. Statistical analysis of TDDB data clearly indicates the presence of bimodal failure distributions indicating the presence of two failure mechanisms. Further investigation is necessary to uncover the nature and physics governing these different failure mechanisms. A three-parameter Weibull model is suggested to be appropriate for modeling Cu-induced TDDB failures where an incubation time exists for Cu out-diffusion.

IC.4 The Characteristics of Cu-Drift Induced Dielectric Breakdown under Alternating Polarity Bias Temperature Stress, *Sung-Yup Jung, Byoung-Joon Kim, Nam Yeal Lee, Baek-Mann Kim, Seung Jin Yeom, Noh Jung Kwak, and Young-Chang Joo*

The breakdown of inter metal dielectric (IMD) under applied electric field has become a significant reliability concern for copper interconnects. The mechanism of dielectric breakdown can be classified as either intrinsic or extrinsic. The intrinsic failure occurs due to its own defects, such as broken bonds or dipole-dipole interaction of defects under applied electric field [1]. The extrinsic failure is attributed to failures induced by extrinsic defects, such as Cu ions migrated from the Cu electrode. Intrinsic failure is important in low-k dielectrics because the bonding in low-k dielectric is weaker than that of SiO2. The device which is operating under high electricfield such as flash memory uses SiO2 as dielectric material. In this case, the intrinsic breakdown is less important but extrinsic failure due to Cu migration through interface between IMD and capping layer is the predominant failure mechanism for TDDB. Conventionally, TDDB test is performed on DC condition, but real device operation is AC rather than pure DC. Therefore, it is important to understand TDDB failures for AC condition. Hwang et al. studied the effect of forward and reverse bias during TDDB using a metal-insulator-semiconductor (MIS) structure. They demonstrated that the migrated Cu ions move back during reverse bias and hence leakage current is recovered by removing the extrinsic defects. However their study uses a MIS structure in which only the metal electrode serves as Cu ion source. In a real damascene interconnect structure, both electrodes are Cu ion sources and therefore the reverse bias effect may be different from that of MIS structure. We studied the Cu migration-induced-failure in damascene and MIS structured Cu/SiO2 interconnects under alternated polarity electric field. AC and DC TDDB tests were performed and their lifetimes were compared. In additon, voltage ramping tests are also preformed on the sample during TDDB tests to study the conduction mechanism during DC and AC TDDB.

IC.5 Electromigration Tests for Critical Stress and Failure Mechanism Evaluation in Cu/W via/Al Hybrid Interconnect, *Zungsun Choi, Byung-Lyul Park, Jong Myeong Lee, Gil-Heyun Choi, Hyeon-Deok Lee, and Joo-Tae Moon*

Electromigration in a hybrid interconnect which consists of copper metallization in via below, aluminum metallization in via above, and tungsten via in between was investigated. Three types of barrier metals for tungsten via were observed. Two failure mechanisms in copper metallization are observed. One type occurs due to void nucleation at the interface between barrier metal of tungsten via and copper. Time to failure highly depends on types of barrier metals. Second type is by void growth in the line. Failure by void growth is *independent* of barrier metal variation, which suggests that the failure is initiated by a defect.

IC.6 Process Options for Improving Electromigration Performance in 32nm Technology and Beyond, *Oliver Aubel, Jörg Hohage, Frank Feustel, Christian Hennesthal, Ulrich Mayer, Axel Preusse, Markus Nopper, Matthias Lehr, Jürgen Boemmels, and Susanne Wehner*

In this paper we present process options to close the gap between electromigration performance needs by design and process performance. We are going to present reliability data for metal capping and advanced copper surface cleaning processes. These processes are showing very good performance and extendibility to 32nm technology nodes and beyond.

IC.7 Joule Heating Effects on Electromigration in Cu/Low-k Interconnects, *Shinji Yokogawa, Yumi Kakuhara, and Hideaki Tsuchiya*

We investigated Joule heating effects on EM in Cu/low-k interconnects. The 1-D radiation mainly contributes to Joule heating. The contribution of the 2-D radiation is larger in a smaller area. However, the passive lines in the same layer do not act as a radiation activator but rather as a compounding factor. EM lifetime degradation is remarkable for dense structure due to poor 2-D radiation. High frequency pulse stress reduces Joule heating, and EM lifetime is improved due to reduction of the Joule heating.

IC.8 Effect of Multiple Via Layout on Electromigration Performance and Current Density Distribution in Copper Interconnect, *Mingte Lin, Nick Jou, James Liang, and K Su*

Downstream Electromigration (EM) was studied on different multiple via structures. Structures with more via gained better EM performance improvement. Failure analysis showed different EM failure modes on these structures. Finite element analysis is applied to find out the current density profiles and their variation between these structures. Resistance increases due to EM induced void are also simulated and found to be dependent on size and location of void. The different EM results of these multiple via structures are explained with the current density results and the different diffusion patterns found.

IC.9 A Novel Test Structure to Study Intrinsic Reliability of Barrier/Low-k, *Larry Zhao, Zsolt Tokei, Gianni Gischia, Marianna Pantouvaki, Kristof Croes, and Gerald Beyer*

A novel test structure to study intrinsic reliability of barrier/low-k is proposed. The structure is based on a planar capacitor design where low-k film is deposited after the patterning of the capacitor, followed by metallization and Cu CMP. This so called low-k planar capacitor structure provides several unique capabilities to study various aspects of barrier/low-k TDDB compared with the conventional damascene structures. Two of the unique capabilities are presented in this paper. First, TDDB from a damage-free low-k material has been measured for the first time using the low-k planar capacitor structure. Second, the test structure is sensitive enough to quantify the impact of selected process conditions, such as barrier re-sputter and plasma treatments, on TDDB.

IC.10 Effects of Photoinduced Carrier Injection on Time-Dependent Dielectric Breakdown, *Joanna Atkin, Robert Laibowitz, Tony Heinz, Jim Lloyd, Thomas Shaw, and Eduard Cartier*

Time-dependent dielectric breakdown experiments were performed under broadband UV illumination in order to investigate the effects of increased electron concentration on time to breakdown. Preliminary results show that breakdown can be achieved at shorter time scales and lower fields than in standard reliability tests.

IC.11 Withdrawn

IC.12 A Comprehensive Look at PVD Scaling to Meet the Reliability Requirements of Advanced Technology, *Roey Shaviv, Sanjay Gopinath, Marcelle Marshall, Tom Mountsier, Girish Dixit, and Yu Jiang*

The reliability of interconnects continues to be a formidable challenge as dimensions shrink from generation to generation. In this paper we demonstrate barrier/seed scaling, enabled by HCM IONX PVD technology. We report high electromigration activation energy of ~ 1 eV, and $J_{max} > 6$ MA/cm^2, exceeding the ITRS 2007 requirements for the next several generations by a wide margin. Thinner barrier/seed with increased barrier etchback is shown to increase electromigration lifetime. Via stress migration results indicate that high barrier etchback is beneficial to reliability. TDDB results show a strong positive effect of barrier etchback on lifetime. We find that breakdown voltage for thinner barrier/seed is higher than that of the control. Breakdown voltage further increases with increased barrier etchback. For TDDB, the field acceleration coefficient, , improves with increased etch back from 3.8 (MV/cm)$^{-1}$ to 5.4 (MV/cm)$^{-1}$ and the expected lifetime at operation conditions is improved by 4 orders of magnitude, exceeding requirements by a wide margin. This comprehensive study of PVD scalability proves a process space that provides the reliability margin necessary for continuing technology scaling for future generations.

IC.13 The Dynamic Thermal Behavior of Silicided Polysilicon Under High Current Stress Event, *Jian Lee, J.R. Shih, David Su, and Kenneth Wu*

A simple dynamic thermal model considering Joule-heating, heat-conduction and energy conservation has been developed. It fits the dynamic thermal behavior of the silicided polysilicon under the high current stress event very well. The criterion to induce the DC resistance change of a silicided polysilicon resistor is determined by the phase transform temperature (PTT) of the silicide polysilicon.

IC.14 Temperature Scaling of Electromigration Threshold Product in Cu/Low-K Interconnects, *Emmanuel Petitprez, Lise Doyen, and David Ney*

In this paper, we report on the temperature dependence of electromigration threshold product in copper interconnects. The electromigration threshold product $(jL)_c$ is first determined from lifetime distributions for temperatures ranging from 260°C to 330°C. We then propose an alternative method to determine $(jL)_c$ at much lower temperatures. We show that the threshold product does not vary significantly in the investigated temperature range. We demonstrate this alternative method is suitable to determine $(jL)_c$ close to the final product operating temperature, which would require unrealistic test duration if performed with a conventional method based on lifetime data.

ME - Micro-Electronic Systems and MEMS Posters

ME.1 Methodology to Analyze Failure Mechanisms of Ohmic Contacts on MEMS Switches, *Adrien Broue, Jérémie Dhennin, Cédric Seguineau, Xavier Lafontan, Christel Dieppedale, Jean-Michel Desmarres, Patrick Pons, and Robert Plana*

This paper demonstrates the efficiency of a new methodology using a commercial nanoindenter coupling with electrical measurement on test vehicles specially designed to investigate the micro contact reliability. This study examines the response of gold contacts with 5 μm^2 square bumps under various levels of current flowing through contact asperities. Contact temperature rising is observed leading to shifts of the mechanical properties of contact material, modifications of the contact topology and a diminution of the time dependence creep effect. The data provides a better understanding of micro-scale contact physics especially failure mechanisms due to the heating of the contact on MEMS switches.

MY - Memory Posters

MY.1 Understanding Barrier Engineered Charge-Trapping NAND Flash Devices With and Without High-K Dielectric, *Hang-Ting Lue, Sheng-Chih Lai, Tzu-Hsuan Hsu, Pei-Ying Du, Szu-Yu Wang, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu*

Barrier engineered charge-trapping NAND flash (BE-CTNF) devices are extensively examined by theoretical modeling and experimental validation. A general analytical tunneling current equation for multi-layer barrier is derived using WKB approximation. The rigorously derived analytical form is valid for both electron and hole tunneling, as well as for any barrier composition. With this, the time evolution (Vt-time) of any BE-CTNF device during programming/erasing can be accurately simulated. The model is validated by experimental results from bandgap-engineered SONOS (BE-SONOS) and various structures using Al_2O_3 top-capping layer. Using this model, various structures of BE-CTNF with high-K tunneling or blocking dielectric are investigated. Furthermore, the low-field tunneling current for various structures are simulated, providing theoretical foundations for retention and read disturb optimization.

MY.2 Study of the Charge-Trapping Characteristics of Silicon-Rich Nitride Thin Films Using the Gate-Sensing and Channel-Sensing (GSCS) Method, *Chi-Pin Lu, Jung-Yu Hsieh, Pei-Ying Du, Hang-Ting Lue, Ling-Wu Yang, Tahone Yang, Kuang-Chao Chen, and Chih-Yuan Lu*

This study investigates the charge trapping characteristics of Si-rich nitride thin films in detail by using the gate-sensing and channel-sensing (GSCS) method. Our results indicate that Si-rich nitride provides higher capture efficiency for thinner nitride, and can enhance the electron de-trapping speed, while at the expense of worse data retention.

MY.3 Statistical Retention Modeling in Floating-Gate Cell: ONO Scaling, *Andrey Serov, Dongwan Shin, Dae Sin Kim, Taikyung Kim, Keun-Ho Lee, Young-Kwan Park, Moon-Hyun Yoo, Tae-hun Kim, Sug-Kang Sung, and Choong-Ho Lee*

The scaling of ONO gate stack in Floating-Gate Memory cell has been analyzed with our developed statistical simulation tool, which allows the modeling of the change of the threshold-voltage distribution in time. The simulation results were compared with measurements on 50nm floating-gate cells. Strong tail behavior in Vth distribution after one week room-temperature retention was observed with the shrinking of the top oxide.

MY.4 Cell Endurance Prediction from a Large-Area SONOS Capacitor, *Chih-Hsiung Lee, W. H. Tu, S. H. Gu, C. W. Wu, S. W. Lin, T. H. Yeh, K. F. Chen, Y. J. Chen, J. Y. Hsieh, I. J. Huang, N. K. Zous, T. T. Han, M. S. Chen, W. P. Lu, K. C. Chen, Tahui Wang, and Chih-Yuan Lu*

Endurance considerations induced by the degradation of top and bottom oxides are proposed for a SONOS memory. First, a correlation is found between the widespread C-V curves induced by interface generation and cycling numbers (cyc. #). Unlike V_{FB} (accumulation region), V_T (inversion region) shows a much severe shift. Interface state (N_{it}) is identified as a key factor even when a 2nm bottom oxide is used. Moreover, charge to breakdown (Q_{BD}) for an ONO capacitor under positive and negative constant current stress (CCS) is investigated. Our study reveals that Q_{BD} of such stacks strongly depends on the top oxide thickness. A field enhancement induced by charges in a trapping nitride layer is the root cause. Based on Weibull statistics, the risk of dielectric breakdown for both blocking layers is then evaluated.

MY.5 Charge Loss Behavior of Manos-Type Flash Memory Cell with Different Levels of Charge Injection, *Man Chang, Minseok Jo, Musarrat Hasan, Seonghyun Kim, Yongkyu Ju, Seungjae Jung, Hyejung Choi, and Hyunsang Hwang*

In this study, we found that the charge loss behavior of MANOS device for NAND Flash memory application is highly dependent on the amount of injected charges (defined as Q_{inj} ($=C_{ox}\times \Delta V_{FB}$)). Beyond the critical amount of Q_{inj} (defined as Q_c), the direction of dominant charge loss path changes from SiO_2 towards Al_2O_3. This result was verified by experimental and simulation results through the comparison between ONO and ONA stacks. For detailed analyses, we investigated the impact of blocking oxide thickness and retention temperature. For further understanding, we performed long-term retention measurements up to $\sim 10^6$ s at different level of Q_{inj} to investigate the correlation between the energy trap level (E_{TA}) and Q_{inj}.

MY.6 A Statistical Model of Erratic Erase Based on an Automated Random Telegraph Signal Characterization Technique, *Andrea Chimenton, Cristian Zambelli, and Piero Olivo*

We propose a new statistical model of the erratic erase based on a new RTS analysis technique. The experimental analysis revealed new interesting features of the erratic erase phenomenon. The overall erased threshold voltage distribution, including tail bits, can be modeled by taking into account the erratic erase behavior whose characteristics can easily be measured by common cycling experiments. The statistical model of the erased threshold voltage obtained in this way can then be used to perform statistical simulation of the bitline leakage current, thus providing a powerful tool in memory design and optimization.

MY.7 Indications for an Ideal Interface Structure of Oxynitride Tunnel Dielectrics, *Ziyuan Liu, Shuu Ito, Takashi Ide, Masashi Nakata, Hirokazu Ishigaki, Mariko Makabe, Markus Wilde, Katsuyuki Fukutani, Hiroyuki Mitoh, and Yoshiaki Kamigaki*

Nitrogen localization in the front of oxide/Si interface is related to a Hydrogen-diffusion barrier. This results in the superior quality of N2O-oxynitride over the NO-oxynitride. We propose that the ideal interface structure of reliable tunnel oxynitride features an N-rich H-diffusion barrier layer in front of the oxynitride/Si interface.

MY.8 Post-Cycling Data Retention Failure in Multilevel Nor Flash Memory with Nitrided Tunnel-Oxide, *Wook Lee, Chang-Hyun Hur, Hyun-Min Lee, Hwanbae Yoo, Sang-Eun Lee, Bong-Yong Lee, Chankwang Park, and Kijoon Kim*

Post-cycling data retention characteristics of a multilevel NOR flash memory with nitrided tunnel-oxide is presented. Results show that retention behavior is strongly related to the amount of interface trap generation rather than that of oxide trap, indicating detrapping from near interface trap is a major factor for threshold voltage shift. Process conditions including nitrogen concentration at the interface and subsequent annealing of nitrided tunnel-oxide by O2 are found to be related to the generation of interface trap and resultant postcyclingretention.

NA - Nanoelectronics Posters

NA.1 Critical Thermal Issues in Nanoscale IC Design, *Lei Jiang, Daniel Pantuso, Per Sverdrup, and Wei-kai Shih*

Silicon process scaling and microprocessor design lead to increasing power density and thermal gradient. A comprehensive methodology is developed to model device to interconnect thermal behavior for architecture pathfinding and reliability verification. This ensures best-in-class reliability by addressing known failure mechanisms such as electromigration and joule heating in design.

PD - Product Qualification Posters

PD.1 Investigation of Chip-Package Interaction - Looking for More Acceleration in Product Qualification Tests, *Werner Kanert and Reinhard Pufall*

Chip-package interaction is a major concern for product reliability. The difference in the thermal expansion of the materials causes mechanical stress that may result in several failure mechanisms such as cracking, interfacial delamination, bond wire break or bond lift-off, and pattern shift. Temperature cycling is a commonly used stress test to address this issue. The paper shows that temperature shock can substitute temperature cycling for certain failure mechanisms, thereby reducing stress times by a factor of 28 or even more. This is especially valuable to reduce development cycles due to faster feedback.

PI - Process and Integration Reliability Posters

PI.1 Reliability of HfO_2/SiO_2 Dielectric With Strain Engineering using CESL Stressor, *Jaechul Kim, Kyong Taek Lee, Seung Hyun Song, Min Sang Park, Seung Ho Hong, Gil Bok Choi, Hyun Sik Choi, Rock Hyun Baek, Hyun Chul Sagong, Yoon-Ha Jeong, Sung Woo Jung, and Chang Young Kang*

We have investigated reliability characteristics for a high-k/metal gate MOSFET with strain engineering under constant voltage stress (CVS). Using contact edge stop layer (CESL), tensile and compressive strains are applied to the channel region. Since the compressive MOSFET has more hydrogen in the CESL, the MOSFET has lower reliability characteristics than others. Though the hydrogen can passivate dangling bonds in the high-k dielectric, the passivated bonds are easily broken by voltage stress, which cause degradation of highk layer.

PI.2 The Role of Nitrogen in HfSiON Defect Passivation, *Robert O'Connor, Marc Aoulaiche, Luigi Pantisano, Adelina Shickova, Robin Degraeve, Ben Kaczer, and Guido Groeseneken*

In this work we examine the effect of nitrogen incorporation on the defect generation behavior in HfSiON gate dielectric layers. We show that nitrogen effectively passivates pre-existing defects in the HfSiO, but the effect is quickly reversed during stress leading to high levels of SILC and NBTI

SE.1 Soft Error Rate Cross-Technology Prediction on Embedded DRAM, *Yi-Pin Fang, Balaji Vaidyanathan, and A. S. Oates*

Embedded DRAM has been widely used in System on Chip (SOC) systems due to its higher density than SRAM. Embedded DRAM soft error rate (SER) has become an important subject since more embedded dynamic random access memories (DRAM) are now embedded on the chip as technology advances. Experiments show alpha-SER rapidly declines with embedded DRAM scaling while neutron-SER is less significantly impacted. We develop a simple and rapid method to predict neutron- and alpha-SER scaling trends for embedded DRAM without the use of complicated simulation procedures.

SE.2 ANITA – A New Neutron Facility for Accelerated SEE Testing at The Svedberg Laboratory, *Alexander Prokofiev, Jan Blomgren, Simon Platt, Ralf Nolte, Stefan Roettger, and Andrey Smirnov*

ANITA (*A*tmospheric-like *N*eutrons from th*I*ck *TA*rget), a new neutron facility for accelerated testing of electronic components and systems for neutron-induced single event effects, has been installed at The Svedberg Laboratory in Uppsala, Sweden. The features of the facility include high LANSCE-equivalent neutron flux, fidelity of the neutron spectrum with regard to the natural environment, flexible size of the beam spot, user flux control, low dose rate from γ-rays, low thermal neutron flux, spacious user area, on-line neutron dosimetry, and possibility to use both white and quasi-monoenergetic beams during the same test campaign. Results of characterization measurements are reported.

SE.3 Role of the Deep Parasitic Bipolar Device in Mitigating the Single Event Transient Phenomenon, *Nobukazu Mikami, Takuya Nakauchi, Akira Oyama, Hajime Kobayashi, and Hiroki Usui*

It was found that the single event transient (SET) phenomenon in logic circuits strongly depends on doping concentrations. We think that two parasitic bipolar devices located under a MOS gate with low channel doping concentration suppress SET. Radiation induced electrons are transferred from a drain to a source. As a result, SET can be reduced without implementing any extra circuit area.

SE.4 Proposal for a New Integrated Circuit and Electronics Neutron Experiment Source at Oak Ridge National Laboratory, *Laura Dominik, Eugene Normand, Michael Dion, and Phillip Ferguson*

Government and customer specifications increasingly require assessments of the single event effects probability in electronics from atmospheric neutrons. The accelerator that best simulates this neutron spectrum is the WNR facility (Los Alamos), but it is underfunded and oversubscribed for present and future needs. A new beam-line is proposed at the Oak Ridge National Laboratory, as part of the Spallation Neutron Source (SNS).

SE.5 Correlation of Soft Error Rates Between Mono-Energetic and Full Spectrum Beams on a 90nm SRAM Technology, *Nayan Patel and Helmut Puchner*

Mono-energetic beams and full spectrum beams have been used for years to calculate the soft error rates of SRAM devices. Each beam type offers advantages and disadvantages, but availability is one of the major issues with full spectrum beams due to limited number of facilities available worldwide. We present correlation data for the newly made available full spectrum ANITA (*A*tmospheric-like *N*eutrons from th*I*ck *TA*rget) neutron beam at TSL, Sweden and the corresponding mono-energetic neutron beam. Single bit and multi bit events on a 90nm SRAM "golden device" are correlated and compared. In addition we also compare the soft error rates to a single 180MeV neutron beam run to further investigate the accuracy of this method. The soft error rates extracted from the different methodologies are comparable and allow the use of the full spectrum ANITA beam for modern SRAM devices.

SE.6 A New Dedicated Neutron Facility for Accelerated SEE Testing at the ISIS Facility, *Christopher Frost, Stuart Ansell, and Giuseppe Gorini*

A new neutron facility for the accelerated testing of electronic components is being designed and built in a joint venture between the Science and Technology Facilities Council (UK) and the Consiglio Nazionale delle Ricerche (Italy) at the ISIS Facility, Rutherford Appleton Laboratory, UK. It aims to help address the increasing demand for neutron facilities of this type and in particular provide neutron test facilities with an atmospheric spectrum extending above 200MeV to 800MeV

TF - Thin Film Devices Posters

TF.1 The Correlation Between Trap States and Mechanical Reliability of Amorphous Si:H TFTs for Flexible Electronics, *M. H. Lee, S. T. Chang, S.-C. Weng, W.-H. Liu, K.-J. Chen, K.-Y. Ho, M. H. Liao, J.-J. Huang, and G.-R. Hu*

The disordered bonds may generate a redistribution of trap states, resulting in unstable electrical characteristics such as threshold voltage, subthreshold swing, and mobility of carriers. The weak or broken bonds may contribute to the redistribution of trap states, and lead to unstable electrical characteristics of the a-Si:H TFTs on plastic substrates. We conclude that the DOS of an a-Si:H layer under mechanical strain is the fundamental reliability issue for the development of flexible electronics.

TF.2 Comparison of Device Degradation of n-Type Metal-Induced Laterally Crystallized Poly-Si TFTs With or Without Hydrogenation, *Mingxiang Wang, Chunfeng Hu, Yan Zhou, and Meijuan Xu*

Hydrogenation effect on reliability of n-type metal-induced laterally crystallized poly-Si TFTs is systematically evaluated by comparing device transfer and output characteristic degradation under both hot carrier (HC) and self-heating (SH) stresses. Under HC stress, hydrogenated device exhibits better stability in transfer characteristics, but worse stability in output characteristics. Under SH stress, hydrogenation leads to instability in both transfer and output characteristics. Under both stresses, very different degradation behaviors associated with hydrogenation are found, reflecting different degradation mechanism involved for hydrogenated devices.

XT - Transistor and BTI and Hot Carrier Posters

XT.1 Studies of NBTI in pMOSFETs with Thermal and Plasma Nitrided SiON Gate Oxides by OFIT and FPM Methods, *W.J. Liu, D. Huang, Q.Q. Sun, C.C. Liao, L.F. Zhang, Z.H. Gan, W. Wong, and Ming-Fu Li*

NBTI in pMOSFETs with plasma (PNO) and thermal (TNO) nitrided SiON gate oxides are re-investigated using our newly developed on-the-fly interface trap (OFIT) and fast pulse *I-V* measurement (FPM) methods. The threshold voltage shift ΔV_{TH} is quantitatively decomposed into interface trap and oxide charge components. It is found that the interface trap generation under stress follows the power law with the same power index n and its temperature dependence. The NBTI degradation in TNO devices is larger than those in PNO devices, particularly the larger component of oxide charge. The result is explained by the different N profile of TNO from that of PNO devices, as supported by the first principle calculation.

XT.2 Layout Dependency of PMOS Off Current Degradation Due to Off-State Stress, *Jae Yong Seo, Hong Sik Park, Sabina Lee, Tae Hun Kang, Gu Gwan Kang, Byung Heon Kwak, and Won Shik Lee*

Off-state hot carrier (HC) stress that is based on MOSFET off leakage current (Ioff) increased after electron trapping is a product reliability concern for DRAM with aggressive short channel length. The previous study described that the standby current (ISC) degradation behavior of the device with shallow trench isolation (STI) is responsible for STI edge trap after burn-in mode operation. In addition, speed problems (speed-up and speed-down) are caused by hot electron or hole tapping during HC stress (Igmax, Ibmax, Vd=Vg stress condition) between narrow width and wide width device as mentioned width dependency. However, Layout dependency of off-state stress degradation of PMOS with STI sidewall trap has not been fully discussed yet. This work focus on trapping characteristics and layout dependency under off-state stress (Vg=high). In order to analyze these behaviors, first, we will isolate the dominant degradation component under dynamic stress (AC) with gate pulsing using inverter circuit. Second, we will depict individual degradation behavior between NMOS and PMOS DC parameters (Id,Vth,Ioff), moreover, will depict how we can obtain information on the deep trap of the sidewall and interface state of STI

top edge of the device by using an adapted hump measure technique. Finally, we will presents that layout related Ioff increase phenomena with finger type gate MOSFET structure and discuss the lifetime extrapolation for both voltage and temperature dependency.

XT.3 Systematic Study on Bias Temperature Instability of Various High-k Gate Dielectrics; HfO_2, HfZrxOy and ZrO_2, *Hyung-Suk Jung, Tae Joo Park, Jeong Hwan Kim, Sang Young Lee, Joohwi Lee, Him Chan Oh, Kwang Duck Na, Jung-Min Park, Weon-Hong Kim, Min-Woo Song, Nae-In Lee, and Cheol Seong Hwang*

HfO_2, $HfZr_xO_y$ and ZrO_2 gate dielectrics are systematically compared in terms of the nMOS PBTI and pMOS NBTI. Compared to HfO_2, ZrO_2 exhibits higher capacitance and superior nMOS mobility characteristics. In addition, as the ZrO_2 content increases, V_{th} shift under the nMOS PBTI stress is dramatically reduced. This is mainly contributed to the lower density of pre-existing bulk traps related to the oxygen vacancies.

XT.4 Theoretical Approach and Precise Description of PBTI in High-k Gate Dielectrics based on Electron Trap in Pre-existing and Stress-Induced Defects, *Junji Shimokawa, Motoyuki Sato, Chikashi Suzuki, Mitsutoshi Nakamura, and Yuzuru Ohji*

We have theoretically analyzed the mechanism of PBTI degradation of high-k gate dielectrics. We proposed a PBTI degradation model based on a comprehensive physical theory using the general notation of gate leakage current and adequate trap distribution. Furthermore, by taking account not only preexistingbut also stress-induced defects, our model could explain the experimental data with high accuracy even though it was very simple. In addition, we have clarified that defect generation rate and/or capture cross-section in HfSiON is different from that in HfLaSiON.

XT.5 Negative Bias Temperature Instability of p-Channel Transistors with Diamond-like Carbon Liner Having Ultra-high Compressive Stress, *Bin Liu, Kian-Ming Tan, Ming-Chu Yang, and Yee-Chia Yeo*

The negative bias temperature instability (NBTI) characteristics of p-channel field-effect transistors with diamondlike carbon (DLC) liner stressor having ultra-high compressive stress (>5 GPa) are investigated for the first time. Ultra-Fast Measurement (UFM) was employed for NBTI study. Power law slopes ranging from ~0.057 to ~0.070 are reported in this work. P-FETs with higher channel strain show greater threshold voltage shift (ΔVth) than those with lower or no channel strain under the same gate voltage VGS stress condition. ΔVth recovery behavior of highly strained devices suggests that both charge trapping and interface trap degradation are enhanced by strain. Despite this, strained p-FETs with Recessed SiGe S/D and DLC stressors are projected to have a NBTI lifetime exceeding 10 years at VG = -1 V, showing no severe reliability issues.

XT.6 Applying the Universal Recovery Equation for Fast Wafer Level Reliability Monitoring NBTI Assessment, *Rolf-Peter Vollertsen, Hans Reisinger, Stefano Aresu, and Christian Schluender*

This work demonstrates that NBTI assessment by fast wafer level reliability methods is possible in a quantitative manner. This involves excluding time periods from the stress time that are used for restoration of damage recovered during stress interruption and a calibrated back extrapolation of measured recovery traces to short delay times based on the universal recovery equation. The development of the methodology, the challenges and the verification of the implemented algorithm are presented.

XT.7 Spin Dependent Recombination Study of the Atomic-Scale Effects of Fluorine on the Negative Bias Temperature Instability, *Jason Ryan, Patrick Lenahan, An Krishnan, Srikanth Krishnan, and Jason Campbell*

Recent work has shown that NBTI can be significantly suppressed by incorporating fluorine in the gate oxide of pure SiO_2 pMOSFETs. We use spin dependent recombination and gated diode current measurements to investigate the atomic-scale processes involved in fluorine's suppression of NBTI. We find that fluorine effectively passivates Si/SiO_2 P_{b0} center precursors, but much less effectively passivates Si/SiO_2 P_{b1} center precursors. Since these defects have significantly different densities of states, our results may be useful in modeling NBTI response in fluorinated oxides. Our results also provide a fundamental explanation for fluorine's ineffectiveness at reducing NBTI in nitrided oxide devices.

XT.8 RF and Hot Carrier Effects in Metal Gate/High-k Dielectric nMOSFETs at Cryogenic Temperature, *Hyun Chul Sagong, Kyong Taek Lee, Seung-Ho Hong, Hyun-Sik Choi, Gil-Bok Choi, Rock-Hyun Baek, Seung-Hyun Song, Min-Sang Park, Jae Chul Kim, Yoon-Ha Jeong, Sung-Woo Jung, and Chang Yong Kang*

We investigate RF performances and hot carrier effects of nMOSFETs at cryogenic temperature. RF performances of HfO_2 dielectric nMOSFET at 77 K are improved more than those of SiO_2 dielectric nMOSFET although DC performances are improved similarly. The nMOSFET with HfO_2 dielectric has 127.4 GHz f_T and 75.4 GHz f_{max} at 77 K. In hot carrier injection measurement, g_m of HfO_2 nMOSFET at 77 K is degraded more than 300 K although V_{th} shift is less. The cause of g_m reduction is discussed related to the trapping.

XT.9 Asymmetry of RTS Characteristics Along Source-Drain Direction and Statistical Analysis of Process-Induced RTS, *Kenichi Abe, Yuki Kumagai, Shigetoshi Sugawa, Shunichi Watabe, Takafumi Fujisawa, Akinobu Teramoto, and Tadahiro Ohmi*

In this work, we investigated random telegraph signal (RTS) amplitude and the probability of trap empty along two different drain current directions for various gate lengths using novel test structures which enable to measure RTS in large numbers. Asymmetry of RTS amplitude along source-drain current direction increases as gate length shortens because a trap near the gate edge dominates RTS phenomenon as gate length shortens. The probability of trap empty shows weak positive correlation between both directions but asymmetric difference of that partially remains. We also investigated RTS characteristics dependence on kinds of gate insulator films and plasma damages of back-end-of-line (BEOL). Silicon oxynitride gate insulator film has bad effect on RTS and plasma damage does not appear as the increase of RTS amplitude up to 51,385 of antenna ratio.

XT.10 Observation of Two Gate Stress Voltage Dependence of NBTI Induced Threshold Voltage Shift of Ultra-Thin Oxynitride Gate P-MOSFET, *Zhiqiang Teo, Diing Shenp Ang, and Guoan Du*

From ultra-fast measurement of NBTI induced threshold voltage shift, we observe two distinct dependence of stress induced defects on the gate stress voltage. The result corroborates an earlier inference, derived from temperature dependence study, that more than one type of defects determines the NBTI of the ultra-thin oxynitride gate p-MOSFET.

XT.11 A New Fast Switching NBTI Characterization Method that Determines Subthreshold Slope Degradation during Stress, *Douglas Brisbin and Prasad Chaparala*

For PMOSFET devices NBTI is a serious reliability concern. Because of recovery effects careful stress and measurement methods must be used to determine threshold voltage (V_T) degradation. These methods typically assume that mobility and subthreshold slope (SS) degradation are minimal. Recent papers have pointed out that this assumption may not be valid. This paper discusses a new fast switching NBTI measurement technique that alternates between two V_{GS} measurement conditions to determine the SS as a function of stress time. In this new method the SS is determined during stress to correctly compensate the V_T degradation for SS degradation. In addition, this paper presents SS and V_T NBTI degradation data from a 2 nm low and high nitrogen and a 6 nm DGO PMOS device to demonstrate the value of this new method.

XT.12 Investigation of Plasma Charging Damage Impact on Device and Gate Dielectric Reliability in 180nm SOI CMOS RF Switch Technology, *Dimitris Ioannou, David Harmon, and Wagdi Abadeer*

We report on plasma induced damage effects on the device and gate dielectric reliability for an SOI CMOS RF Switch technology. Although no early gate dielectric failures are detected from voltage breakdown measurements, detrimental antenna effects are observed on the NBTI performance. NBTI recovery effect is observed for the antenna devices, but it is found to be reduced relative to the recovery obtained for devices with low antenna effects.

XT.13 Positive and Negative Bias Temperature Instability in La_2O_3 and Al_2O_3 Capped High-k MOSFETs, *Marc Aoulaiche, Ben Kaczer, Moonju Cho, Michel Houssa, Robin Degraeve, Thomas Kauerauf, Amal Akheyar, Tom Schram, Philippe Roussel, Herman Maes, Thomas Hoffmann, Serge Biesemans, and Guido Groeseneken*

PBTI and NBTI reliability is investigated on La2O3 and Al2O3 capped n and pMOSFETs, respectively. Low Vth devices are achieved using the capping layers without degrading BTI reliability. For the Al2O3 capped pMOSFETs no additional defects related to the capping are observed. The La2O3 capping layer for nMOSFETs induces shallow traps, which however are not critical at operating conditions.

XT.14 Effect of Mechanical Strain on the NBTI of Short-Channel P-MOSFETS : Role of Impact Ionization, *Zhiqiang Teo, Diing Shenp Ang, Kwang Seng See, and Pei Zhen Yang*

Stressed induced degradation of mechanically strained short-channel p-MOSFETs is shown to be particularly sensitive to the hot-hole effect triggered by impact ionization at high gate voltage stress, but not to the cold holes present at typical stress voltage employed for NBTI. This result is key to reconciling current controversies on the role of mechanical strain on NBTI.

XT.15 Frequency and Recovery Effects in High-k BTI Degradation, *Stephen Ramey, Chetan Prasad, Marty Agostinelli, Sangwoo Pae, Steven Walstra, Satrajit Gupta,and Jeffrey Hicks*

Net end-of-life aging prediction under realistic use conditions is the key objective for any product aging model. In this paper, a net degradation model is introduced and effects such as recovery, subsequent degradation, frequency, duty cycle, and recovery bias are evaluated. The high-k recovery behavior observed is consistent with SiO_2 gate stacks, which allows the use of SiO_2 models to predict recovery in both NMOS and PMOS high-k transistors.

XT.16 New Insights into the Wide I_D Range Channel Hot-Carrier Degradation in High-k Based Devices, *Esteve Amat, Rosana Rodríguez, Montserrat Nafría, Xavier Aymerich, Thomas Kauerauf, Robin Degraeve, and Guido Groeseneken*

At low energy range, the Lucky Electron Model does not describe correctly the Channel Hot-Carrier (CHC) degradation for transistors with both SiO_2 and high-k dielectric. A new picture to explain the CHC degradation behavior in nMOSFETs based on the dominant role of the gate voltage into the total CHC stress is presented.

XT.17 Do NBTI-Induced Interface States Show Fast Recovery? A Study Using a Corrected On-The-Fly Charge-Pumping Measurement Technique, *Philipp Hehenberger, Thomas Aichinger, Tibor Grasser, Wolfgang Gös, Oliver Triebl, Ben Kaczer, and Michael Nelhiebel*

Data obtained by the recently developed on-the-fly chargepumping technique has suggested a fast initial degradation and recovery of interface states during negative and/or bias temperature stress, contrary to previously published results. By revising the analysis of the measurement setup, fast interface state creation and recovery are revealed as artifact due to a different amount of oxide traps seen during the stress and relaxation phases. From this analysis we conclude that data gathered during stress and recovery phases must not be directly compared. By properly taking the contribution of (slow) oxide charges into account, which leads to a spurious increase of the charge-pumping current during the stress phase, we demonstrate that no fast initial degradation and no fast recovery of interface states occurs. Nevertheless, the charge-pumping signal is sensitive to the continuous switching of the gate voltage into accumulation, which also accelerates interface state recovery, albeit at a slower rate. We finally conclude that both the fast initial degradation and the fast initial recovery seem to be due to oxide charges. Therefore these oxide charges need to be considered. By performing simulations with our device simulator Minimos-NT using a modified Shockley-Read-Hall model it was possible to reproduce the effect of these oxide charges. For this purpose a temperature and field activated tunneling process is assumed and results in proper agreement of measurement and simulation. A correction scheme for the on-the-fly charge-pumping measurement technique is then presented.

THURSDAY MORNING
April 30, 2009

Session 5A: Interconnect Electro- and Stress-Migration
Le Grand Salon, 8:15 am
Chair: Baozhen Li, IBM and Vice Chair, Armin Fischer, Infineon

5A.1 (Invited) Thermomechanical Reliability for Emerging Device Technologies: Implications for ULK Integration, 3-D Structures and Packaging, *Reinhold Dauskardt*

In this paper, the reliability requirements, thermal behaviour and failure mechanisms of solidly mounted Bulk Acoustic Wave (BAW) filters are studied. High power RF stress measurements are presented where the evolution of the surface damage of the BAW filters as a function of stress time is analysed by optical height profiling. Two different metal stacks were used. The main failure mechanism for BAW filters during high RF power stress is proposed to be acoustomigration. By comparing the stress measurements to the requirements, excellent reliability of NXP's BAW duplexers is proven.

5A.2 The Effect of a Threshold Failure Time and Bimodal Behavior on the Electromigration Lifetime of Copper Interconnects, *Ronald Filippi, Ping-Chuan Wang, Andy Brendler, Paul McLaughlin, Jim Poulin, Bruce Redder, Jim Lloyd,and James Demarest*

Electromigration results are described for a Dual Damascene structure with copper metallization and a low-k dielectric material. The failure times follow a bimodal lognormal behavior with early and late failures. Moreover, there is evidence of a threshold failure time such that each failure mode is represented by a 3-parameter lognormal distribution. It is found that the threshold failure time scales differently with current density from the median time to failure, which can be explained by considering two components of the electromigration lifetime: one controlled by void nucleation and the other controlled by void growth.

5A.3 Void Nucleation and Growth Contributions to the Critical Current Density for Failure of Cu Vias, *Anthony Oates and Ming-Hsien Lin*

We investigate the critical current density for electromigration failure, jc, as a function of voiding failure mode for Cu dual damascene vias. We demonstrate experimentally the variation of (jL) product with via failure mode showing that it is not possible to characterize vias by a single (jL). We suggest that, in general, jc for failure is determined by the sum of void nucleation and growth components, and we present a model for jc based on these concepts.

5A.4 Time and Temperature Dependence of Early Stage Stress-Induced-Voiding in Cu/Low-k Interconnects, *Kristof Croes, Chris J. Wilson, Melina Lofrano, Youssef Travaly, David De Roest, Zsolt Tőkei, and Gerald P. Beyer*

The time and temperature dependence of Stress-Induced-Voiding below and in copper VIA's with a diameter of 80nm integrated in a k=2.5 material was studied. The focus was on the early phase of the voiding process. To accelerate the degradation, test structures with big metal plates below and/or above the VIA were used. We found two degradation mechanisms in which one dominated below and the other dominated above a certain temperature. The first mechanism has an activation energy of 0.9eV and is the result of interface-diffusion driven by a stress-gradient. This mechanism was more pronounced below the VIA, but was significant in the VIA as well. The second mechanism has an activation energy of 1.2eV, which is argued to be driven by grain boundary diffusion due to a vacancy gradient in and above the VIA. To explain both mechanisms, an addition to the traditional stress-creep model is proposed and fits our data well. Additionally, it is discussed that VIA's connected to the center of big metal plates above and below the VIA are less susceptible to SIV compared to VIA's connected to line ends either below or on top of the VIA. We support our argumentation and analytical modeling with Finite Element Modeling.

Session 5B: Interconnect Low-k
Le Grand Salon, 10:25 am
Chair: Baozhen Li, IBM and Vice Chair: A.S. Oates, TSMC

5B.1 Critical Ultra Low-*k* TDDB Reliability Issues For Advanced CMOS Technologies, *Fen Chen, Michael Shinosky, Baozhen Li, Jeffrey Gambino, S. Mungeon, P. Pokrinchak, John Aitken, Dinesh Badami, Matthew Angyal, Ravi Achanta, Griselda Bonilla, Guoyong Yang, Guoyong Yang, Pan Liu, K. Li, J. Sudijono, Y. Tan, T.J. Tang, C. Child*

As the technology advances, several critical ULK TDDB issues were faced for the first time and needed to be addressed. First, the increase of ULK leakage current noise level induced by soft breakdown during stress was observed. Second, it was found that ULK had lower field acceleration than dense low-*k*. Such process and material dependences of ULK TDDB kinetics were investigated, and an optimal process to improve ULK voltage acceleration was identified. Last, a systematic study of via TDDB regarding area scaling and test structure design was conducted. It was found that only a portion of the total vias possibly determines the low-*k* via TDDB. A new "fatal" via ratio concept is introduced to replace the as-designed area ratio for TDDB area scaling in structures with vias, and a methodology called shift and compare (S&C) is proposed to determine the "fatal" via ratio.

5B.2 New Perspectives of Dielectric Breakdown in Low-*k* Interconnects, *Kok Yong Yiang, Walter Yao, Amit Marathe, and Oliver Aubel*

An alternative method of analyzing time-dependent dielectric breakdown (TDDB) data for low-*k* dielectrics is presented. The analysis shows that time to breakdown is well correlated to the Poole-Frenkel emission equation, and therefore the $\sqrt{E}$-model is a more accurate model in describing the TDDB physics for low-*k* BEOL dielectrics.

5B.3 Fundamental Understanding of Porous Low-K Dielectric Breakdown, *Shou-Chung Lee, A. S. Oates, and Kow-Ming Chang*

We investigate the impact of porosity on the reliability of low-k dielectrics. We show that electric field enhancement around pores occurs and is significantly increased by Cu interaction, suggesting a new potential mechanism for breakdown of dielectrics at stress conditions. We develop of an analytic model to predict failure distribution parameters as a function of porosity and show that the model is in good agreement with measurements for porosity in the range of 5% to 40%. We explain why the field acceleration factor γ is a constant for all silica-based material according to percolation theory. We propose that the percolation path difference between high field and low field would make the field dependence on failure time become non-linear.

Session 5C: High-k Gate Dielectric: SILC and Breakdown
Marquette/Jolliet Rooms, 8:15 am
Chair: Sangwoo Pae, Intel

5C.1 Stress-Induced Leakage Current and Defect Generation in nFETs with HfO_2/TiN Gate Stacks During Positive Bias Temperature Stress, *Eduard Cartier and Andreas Kerber*

The stress-induced leakage current (*SILC*) in nFETs with SiO_2/HfO_2 dual-dielectric gate stacks and TiN electrodes is studied during positive bias temperature stress at high temperatures and at high gate stress voltage. It is shown, that strong defect creation in the HfO_2 causes a linear increase of the *SILC* with stress time. The generated defects are attributed to oxygen vacancies in the HfO_2 layer. The reliability implications of this defect creation phenomenon are discussed.

5C.2 Evidence of a New Degradation Mechanism in High-k Dielectrics at Elevated Temperatures, *Sahar Sahhaf, Robin Degraeve, Robert O'Connor, Ben Kaczer, Mohammed Zahid, Philippe Roussel, Luigi Pantisano, and Guido Groeseneken*

Elevated temperatures can significantly affect the driving forces of high-k degradation and breakdown. Okada *et al.* have proposed the Generated Subordinate Carrier Injection model. This model claims the universality of Stress-Induced Leakage

Current vs. hole fluence, independent of the temperature in n-channel MOSFET's with Hf and Al-based gate dielectrics. We demonstrate that 125°C is a crucial temperature for the studied stack as an additional degradation mechanism is triggered above this temperature. We study the T-dependent energy spectrum of the generated defects and prove that the generation rate and the kind of participating traps in the breakdown path change at elevated temperatures.

5C.3 Characterization of SILC and Its End-of-Life Reliability Assessment on 45nm High-K and Metal-Gate Technology, *Sangwoo Pae, Tahir Ghani, Mike Hattendorf, Jeff Hicks, Jason Jopling, Jose Maiz, Kaizad Mistry, Jim O'Donnell, Chetan Prasad, Jami Wiedemer, and Jason Xu*

Stress Induced Leakage Current (SILC) has been observed on non-optimized high-K (HK) and metal-gate (MG) transistors. Large NMOS PBTI degradation and correlation to SILC increase on such gate stack is a result of large trap generations in the bulk-HK. This poses a long term reliability concern on product standby power and can limit the operating voltage if not suppressed. On an optimized HK+MG process, we demonstrate that SILC has been suppressed. The transistor level SILC data, model and Product burn-in stress data support this. Withoptimized process, SILC has no impact on products made of 45nm HK+MG transistors.

5C.4 TDDB Failure Distribution of Metal Gate /High-k CMOS Devices on SOI Substrates, *Andreas Kerber, Eduard Cartier, Barry Linder, Siddarth Krishnan, and Tanya Nigam*

Extensive breakdown measurements with large statistic confirm that the TDDB failure distribution follows Poisson area scaling. However, towards larger areas and lower failure percentiles the distribution changes in ways similar to those reported for progressive breakdown in poly Si / SiON gate stacks. The change in failure distribution is found to be more pronounced for nFET than for pFET devices. In addition AC TDDB testing was explored, confirming the shape of the DC failure distributions but shows a significant reduction in TDDB lifetime for nFET devices.

Session 5D: Gate Breakdown and Transistor Hot Carriers

Marquette/Jolliet Rooms, 10:25 am
Chair: Sangwoo Pae, Intel and Vice Chair: Vincent Huard, STMicroelectronics

5D.1 The Effect of Interface Thickness of High-k/Metal Gate Stacks on NFET Dielectric Reliability, *Barry Linder, Eduard Cartier, Siddarth Krishnan, James Stathis and Andreas Kerber*

This paper explores the trade-offs of interface layer (IL) thickness, interface growth process, and interface nitrogen content on NFET dielectric reliability using ramp breakdown tests. The median breakdown voltage and the Weibull slope correlate strongly with the gate leakage irrespective of the IL process. Both reliability parameters are predominately modulated by the IL thickness.

5D.2 Description of Si-O Bond Breakage Using Pair-Wise Interatomic Potentials Under Consideration of the Whole Crystal, *Stanislav Tyaginov, Wolfgang Gös, Tibor Grasser, Viktor Sverdlov, Philipp Schwaha, Rene Heinzl, and Franz Stimpfl,*

We extend the McPherson model in a manner to capture the effect of the whole surrounding lattice on the silicon-oxygen bond-breakage energetics. It is shown that the Mie-Grüneisen potential with the constants used in the original version of the model is not suitable under the consideration of the whole crystal. Other empirical pair-wise interatomic potentials, namely TTAM and BKS have been tested for the analysis of the bond rupture energetics. It is shown that the secondary minimum corresponding to the transition of the Si atom from the 4-fold to the 3-fold coordinated position occurs in a different direction with a rather high activation energy (~ 6 eV). The tunneling of the Si ion between the primary and the secondary minima has been treated within the WKB approximation. We demonstrate that the contribution of neighboring SiO_4 tetrahedrons substantially decreases the breakage rate, making bond rupture by means of an electric field alone practically impossible. Therefore, the common action of an electric field and another contribution (bond weakening by hole capture, structural disorder and energy deposited by particles) is essential for Si-O bond-breakage.

5D.3 Accurate Model for Time-Dependent Dielectric Breakdown of High-k Metal Gate Stacks, *Tanya Nigam, Andreas Kerber, and Peter Peumans*

Time-dependent dielectric breakdown (TDDB) in high-k (HK) dielectric stacks is characterized by short breakdown times and shallow Weibull slopes. In this work, these observations are explained by a percolation model with different defect generation rates in the HK layer and interfacial SiO_x layer that form the stack. The difference in defect generation rate impacts the statistics of breakdown of the stack and bimodal distributions are obtained with a transition from a shallow to steep Weibull slope for large areas. It is shown that for a HK layer with a low initial defect density, long breakdown times and steep Weibull slopes are obtained for typical product areas, mitigating TDDB as a reliability show-stopper for HK dielectrics.

5D.4 Hot-Carrier Acceleration Factors for Low Power Management in DC-AC Stressed 40nm NMOS Node at High Temperature, *Alain Bravaix, Chloé Guerin, Vincent Huard, David Roy, Julien-Marc Roux, and Emmanuel Vincent*

Channel Hot-Carrier degradation presents a renewed interest in the last NMOS nodes where the device reliability of 40nm and Input/Output device is difficult to achieve at high temperature as a function of supply voltage and back bias. A three mode interface trap generation is proposed based on the energy acquisition involved in distinct interactions in all V_{GS}, V_{DS} (V_{BS}) conditions as a single I_{DS} lifetime dependence is observed with V_{GD}. This gives a new age(t) function for accurate DC to AC transfers. Positive temperature activation is explained by the rise of ionization rate with electron-electron scattering (medium I_{DS}) and multi vibrational excitation (higher I_{DS}) which increase the H desorption by thermal emission.

Session 5E: MEMS

Duluth/Mackenzie Rooms, 8:15 am

Chair: Paul van der Wel, NXP and Vice Chair: David Grosjean, Analog Devices

5E.1 Repeatability Study of an Electrothermally Actuated Micromirror, *Sagnik Pal and Huikai Xie*

With their large scan range and low drive voltages, electrothermally-actuated micromirrors have great potential in optical biomedical imaging applications, but the repeatability and reliability of such micromirrors are not well understood. This paper reports the conditions for achieving repeatability of the embedded resistive heater and the mirror tilt angle of an electrothermal bimorph micromirror. The upper limit of the actuation voltage that does not degrade the embedded heater performance has been established. A mechanism has been proposed to explain device failure at high actuation voltages. Localized hot-spots in the embedded resistive heater are found to be the root cause of failure.

5E.2 Thermal Behavior and Reliability of Solidly Mounted Bulk Acoustic Wave Duplexers under High Power RF Loads, *Paul van der Wel, Olaf Wunnicke, Frank de Bruijn, and Remco Strijbos*

In this paper, the reliability requirements, thermal behaviour and failure mechanisms of solidly mounted Bulk Acoustic Wave (BAW) filters are studied. High power RF stress measurements are presented where the evolution of the surface damage of the BAW filters as a function of stress time is analysed by optical height profiling. Two different metal stacks were used. The main failure mechanism for BAW filters during high RF power stress is proposed to be acoustomigration. By comparing the stress measurements to the requirements, excellent reliability of NXP's BAW duplexers is proven.

5E.3 Reliability Characterization of Interconnects in CMOS Integrated Circuits Under Mechanical Stress, *Stefan Hillebrecht, Ilia Polian, Bernd Becker, Patrick Ruther, Stanislav Herwik, and Oliver Paul*

CMOS IC interconnects between metallization and silicon are particularly challenged by mechanical stress. We characterize the reliability of these interconnects using a novel CMOS-based MEMS component. Initial experiments provide somewhat unexpected insight into patterns of failure of different types of interconnect.

5E.4 ESD Stress in RF-MEMS Capacitive Switches: The Influence of Dielectric Material Deposition Method, *Jinyu Ruan, George Papaioannou, Nicolas Nolhier, Marise Bafleur, Fabio Coccetti, and Robert Plana*

The present work investigates the influence of dielectric film deposition method on the charging behavior of RF-MEMS capacitive switches, stressed by electrostatic discharges. A Transmission Line Pulsing generator is used to produce the short transient event. The results show two simplified charging mechanisms influenced by discharges. The comparison between two silicon nitride confirms the effect of the dielectric material deposition method on the reliability of the switches.

Session 5F: Late Papers and ESD
Duluth/Mackenzie Rooms, 10:25 am
Chair: Christian Russ, Infineon

5F.1 New On-Chip Screening Of Gate Oxides In Smart Power Devices For Automotive Applications, *Vezio Malandruccolo, Mauro Ciappa, Hubert Rothleitner, and Wolfgang Fichtner*

Efficient screening procedures for the control of the gate oxide defectivity are vital to limit early failures especially in critical automotive applications. Traditional strategies based on burn-in and in-line tests are able to provide the required level of reliability but they are expensive and time consuming. This paper presents a novel approach to the gate stress test of Lateral Diffused MOS transistors based on an embedded circuitry that includes logic control, high voltage generation, and leakage current monitoring. The concept, advantages and the circuit for the proposed built-in gate stress test procedure are described in very detail and illustrated by circuit simulation.

5F.2 Embedded PowerPC 405 & 440-Based SoC Product Qualifications on 45°-Rotated Substrates, *Pascal Nsame, George Tang, Ernie Viau, Khambay Outama, Teddy Nigussie, Claude Dunston, Edward Sziklas, George Goth, and Carole Graas*

We discuss functionality, performance, power and reliability evaluations of the world's first SoC products fabricated using IBM 90nm technology on a 45°-rotated substrate. We have demonstrated reliable product operational lifetimes with up to 12% improved across die delay variability including 30% product performance improvement and 33% leakage reduction over non-rotated substrate.

5F.3 Prediction of Gate Dielectric Breakdown in the CDM Timescale Utilizing Very Fast Transmission Line Pulsing, *David Ellis, Slavica Malobabic, Juin Liou, and Jean-Jacques Hajjar*

In this paper, prediction of Gate Oxide Breakdown (GOB) in the Charged Device Model (CDM) timeframe is performed. The prediction does not require lengthy low-voltage Constant Voltage Stress (CVS) measurements but instead utilizes short (less than 5 seconds per measurement) high-voltage CVS measurements as well as quick Ramped Voltage Stress (RVS) measurements to calculate a voltage to breakdown (*VBD*) in the CDM timeframe as well as the dispersal of actual TDDBs for each oxide area and thickness. To this end, a modified form of the Power Law, called the Trapezoidal Power Law, is derived to simplify data processing and allow comparisons between RVS and CVS. The prediction methodology using the Trapezoidal Power Law is finally demonstrated to predict the exact voltage required to consistently damage the oxide within a single pulse.

5F.4 Field Effect Diode for Effective CDM ESD Protection in 45 nm SOI Technology, *Shuqing Cao, Stephen Beebe, Akram Salman, Mario Pelella, Jung-Hoon Chun, and Robert Dutton*

The improved field-effect diode (FED) has been characterized and modeled in 45 nm SOI technology. It is experimentally shown to be suitable for pad-based local clamping ESD protection. Usual V_{dd} (1V) satisfies the forward-blocking requirement during normal operation. ESD capabilities are investigated using very fast transmission line pulse (VF-TLP) tests to evaluate the device's performance in charged device model (CDM) ESD events. The FED's advantages in improving transient turn-on behavior and reducing DC leakage current have been analyzed. Technology CAD (TCAD) simulations are used to interpret the turn-on behavior and the physical effects. Process tradeoffs have been evaluated.

Session 6A: Interconnect Dielectric Breakdown
Le Grand Salon, 1:40 pm
Chair: Armin Fischer, Infineon and Vice Chair: Fen Chen

6A.1 On the Contribution of Line-Edge Roughness to Intralevel TDDB Lifetime in Low-k Dielectrics, *Jim Lloyd, Xiao-Hu Liu, Griselda Bonilla, Tom Shaw, Eric Liniger, and Anthony Lisi*

A TDDB reliability experiment was performed on interdigitated comb structures with intentionally severe line-edge roughness and the results were then compared to a simple theoretical model. It is seen that for the case studied, the predictions of the model do not compare well to the experimental data, but that for some observed cases the effect of reducing spacing between lines is so strong that more substantial defects must be invoked as a source of failure.

6A.2 Copper Line Topology Impact on the SiOCH Low-k Reliability in Sub 45nm Technology Node. From the Time-Dependent Dielectric Breakdown to the Product Lifetime, *Maxime Vilmay, David Roy, Cedric Monget, Fabien Volpi, and Jean-Marc Chaix*

SiOCH low-k dielectrics introduction in copper interconnects associated to the critical dimensions reduction in sub 45nm technology nodes is a challenge for reliability engineers. Circuit wear-out linked to low-k dielectric breakdown is now becoming a major concern. With the reduction of the line to line spacing, the control of the copper line topology is becoming a first order parameter governing the low-k dielectric reliability. Improving the low-k reliability requires to discriminate each topological effect and quantify its impact on the lifetime at product level. This paper demonstrates the importance of the copper line shape, of the line edge roughness (LER) and of the median line to line spacing variation within the wafer on the low-k dielectrics reliability. Moreover, simple analytical models are described to quantify each effect on the Time-Dependant Dielectric Breakdown (TDDB) and particularly on the final product lifetime. Some advices are given to avoid erroneous lifetime projection.

6A.3 Effect of Chemical Mechanical Polishing Scratch on TDDB Reliability and its Reduction in 45nm BEOL Process, *Wei Liu, Yeow Kheng Lim, Fan Zhang, Wenyi Zhang, Changqing Chen, Bei Chao Zhang, Juan Boon Tan, Dong Kyun Sohn, and Liang Choo Hsia*

The correlation of time-dependent dielectric breakdown (TDDB) reliability failure with scratches generated from chemical mechanical polishing (CMP) in 45nm backend-of-line (BEOL) process is investigated. The wafer map of early TDDB failure samples matches well with the defect wafer map from bright field scans. Electrical fault isolation using thermally induced voltage alteration (TIVA) analysis is employed to locate the hot spot where TDDB leakage occurs. Polish scratch-induced metal damage at the hot spot is further analyzed by top-down scanning electron microscopy (SEM) after de-processing. Also, the depth of the polish scratch is confirmed by using transmission electron microscopy (TEM) analysis. It clearly shows that the embedded particle on copper (Cu) surface and the liner damage resulted from polish scratch severely affect the TDDB reliability. In-situ CMP platen3 (P3) pad chemical pre-clean is found to reduce the polish scratch density effectively and significantly improve the V-ramp/TDDB reliability performance. However, inappropriate usage of chemical pre-clean would cause Cu corrosion and lead to EM degradation. Hence, a balance between polish scratch reduction and Cu corrosion associated with P3 pad pre-clean needs to be achieved.

6A.4 An Efficient Approach to Quantify the Impact of Cu Residue on ELK TDDB, *M.N. Chang, C.J. Wang, C.C. Chiu, and Kenneth Wu*

In this study, Triangular Voltage Sweep (TVS) is shown to be an effective way for quantifying the amounts of free Cu ions in porous low-k film. Free Cu ions at the interface that correlate with the Inter-Metal Dielectric (IMD) TDDB lifetime is also discussed. Adding a thermal treatment after the Chemical Mechanical Polish (CMP) process shows that the IMD TDDB lifetime can be improved by at least 2 orders of magnitude with a decrease in Cu ions at the interface. This study also proves that the TVS method can be used to evaluate Cu ions as well as Time of-Flight Secondary Ion Mass Spectrometry (TOFSIMS).

Session 6B: Circuit Reliability

Marquette/Jolliet Room, 1:40 pm
Chair: Vincent Huard, STMicroelectronics and Vice Chair: Subhasish Mitra, Stanford University

6B.1 CMOS Device Design-in Reliability Approach in Advanced Nodes, *Vincent Huard, C.R. Parthasarathy, A. Bravaix, C. Guerin, and E. Pion*

A general framework is proposed to characterize digital library gates for NBTI and HCI ageing effects. Required parameters extraction is demonstrated for practical cases using accurate, state-of-the-art reliability simulation flow. Both NBTI recovery and HCI models are required to accurately assess digital product degradation

6B.2 Accurate Product Lifetime Predictions Based on Device-Level Measurements, *Tanya Nigam, Biju Parameshwaran, and Gernot Krause*

Product level lifetime margins, determined by HCI and BTI, are shrinking with scaling. We developed highly accurate device-level HCI degradation models that, together with known BTI models, are able to accurately predict frequency degradation of a ring oscillator. We show that despite substantial relief from HCI damage in balanced switching circuits, HCI degradation still accounts for 40-50% of frequency degradation for a 10-year product life.

6B.3 Mapping Systematic and Random Process Variations Using Light Emission from Off-State Leakage, *Franco Stellari, Peilin Song, Alan Weger, and Darrell Miles*

In this paper, we present for the first time the use of an optical imaging technique that we have developed to map systematic and random variability effects across several phases of development of a new microprocessor chip fabricated with the latest IBM SOI 65 nm technology. The technique relies on the detection and subsequent analysis of the Light Emission from Off-State Leakage Current (LEOSLC) by means of static imaging cameras, mounted on a microscope or other optical collection optics. The variability maps created using this method are very simple to generate and have been successfully verified by comparing them to data obtained by on-chip electrical sensors such, as Process Sensitive Ring Oscillators (PSROs), power supply currents, and test results. The visual representation is very helpful in picking up systematic effect and to measure the correlation distance of the variations.

6B.4 Experimental Study Of Gate Oxide Early-Life Failures, *Tze Wee Chen, Young Moon Kim, Kyunglok Kim, Yoshio Kameda, Masayuki Mizuno, and Subhasish Mitra*

Large-scale experimental data from 90nm test chips consisting of 49,152 transistors, and experiments on 90nm test chips containing inverter chains are used to establish: 1. A gate-oxide early-life failure (ELF, also called infant mortality) candidate transistor produces gradually degraded drive currents over time; 2. A digital circuit path consisting of a gate-oxide ELF candidate transistor experiences gradual delay shifts over time before the circuit produces functional failures. These results may be utilized to effectively overcome ELF challenges in scaled CMOS technologies.

Session 6C: ESD

Duluth/Mackenzie Rooms, 1:40 pm
Chair: Christian Russ, Infineon

6C.1 Breakdown Voltage Walkout Effect in ESD Protection Devices, *David LaFonteese, Vladislav Vashchenko, and Konstantin Korablev*

Using experimental and numerical simulation analysis the breakdown voltage walkout effect has been studied in 40 V ESD protection devices based on extended drain MOS devices implemented in a 5 V CMOS process. A similar effect has been observed in 100 V and 24 V BiCMOS processes. The physical mechanism of this effect is revealed as the result of hot electron

capture in the thick field oxide of the extended drain region. To address this, a method to reduce the walkout effect in high voltage ESD devices is proposed and experimentally validated.

6C.2 A Novel ESD Protection Device Structure for HV-MOS ICs, *Tsutomu Imoto, Kouzou Mawatari, Kuniko Wakiyama, Toshio Kobayashi, Motoyasu Yano, Mamoru Shinohara, Takashi Kinoshita, and Hisahiro Ansai*

A novel lateral bipolar ESD protection device is proposed for 16V-DEMOS ICs. This device features a shallow n^+ ballast region between the drift region and the drain region. Due to this ballast region, avalanche generation occurs both in this ballast region and in the drain region. This distributed avalanche generation reduces current crowding at the drain edge. Consequently, this device suppresses soft leakage degradation and provides excellent scalability of MM/HBM failure voltage with gate width. To our knowledge, this is the first report of high-voltage lateral bipolar device without a buried n+ layer to offer such design and performance qualities.

6C.3 A New Physical Insight and 3D Device Modeling of STI Type DENMOS Device Failure Under ESD Conditions, *Mayank Shrivastava, Jens Schneider, Maryam Baghini , Harald Gossner, and V. Ramgopal Rao*

We present experimental and simulation studies of STI type DeNMOS devices under ESD conditions. The impact of base-push-out, power dissipation because of space charge build-up and, regenerative NPN action, on the various phases of filamentation and the final thermal runaway is discussed. A modification of the device layout is proposed to achieve an improvement (~2X) in failure threshold (I_{T2}).

6C.4 The Mechanism of Device Damage During Bump Process For Flip-Chip Package, *Jian Lee, J.R. Shih, Chin Tang, Pao Niu, D-J Perng, Y-T Lin, David Su, and Kenneth Wu*

Ring-type yield loss at wafer edge has been observed during flip-chip packaging process. The failure mechanism is attributed to the scrubber clean process step which generates a lot of charges. This in turn behaves like an electrostatic discharge (ESD) event and damages gate oxide of internal circuits. An equivalent circuit is proposed to analyze such a kind of ESD event and proves the importance of the parasitic capacitance of the interconnect metal.