Session 2A: Gate Dielectrics
Chair: Paul Nicollian, Texas Instruments
Co-Chair: Yuichiro Mitani, Toshiba

10:05 a.m.
Session Introduction

10:10 am

Progressive breakdown and multiple Breakdown are unequivocally observed with thin and thick stacks for all stress conditions investigated. Unlike SiON films, we found the residual timed distributions of high-k stacks exhibit shallow slopes. With long-term module stress (> 5 months), we reported an increased voltage acceleration factor in contrast to that of SiON. Our results are critical to resolve the discrepancy between product data and 1st BD model prediction reported recently for high-k stacks with the implementation of a realistic circuit TDDB methodology.

10:35 a.m.

In sub-1nm EOT high-k/metal gate nMOS, the conventional softbreakdown based TDDB lifetime extrapolation fails. The wearout phase has to be included in the extrapolation and in this paper we present 3 different methods for experimental determination of the necessary softbreakdown and wearout parameters from 1) tSBD & tHBD 2) HBD-only and 3) SILC & tHBD measurements, and discuss their respective advantages and disadvantages.

11:00 a.m.
2A-3 Frequency Dependent TDDB Behaviors and its Reliability Qualification in 32nm High-k/Metal Gate CMOSFETs, K. T. Lee, J. Nam, M. Jin, K. Bae, J. Park, L. Hwang, J. Kim, H. Kim and J. Park, Samsung Electronics

The propensity of TDDB behaviors of HK/MG CMOSFETs on DC and AC stress conditions is considered in comparison to poly-Si/SiON. Although HK/MG nMOSFETs with bipolar AC stress exhibit shorter tbd than with DC in a lower frequency because of hole trapping into IL, bipolar stress in high frequency shows longer tbd than DC. As such AC based TDDB would not be a major concern for technology process qualification for HK/MG technology

1:25 a.m.

Gate oxide breakdown (BD) has been studied in the circuit-like patterns, i.e. e-Fuse arrays and two-stage inverter circuit. The stressed device will suffer only soft BD not a hard BD and it is independent with the current drive capability of current limiting transistors. Circuit functionality will be immune from gate oxide BD in normal circuit operating condition and designers will get extra reliability margin. Our HSPICE simulation results on ring oscillator also suggest the circuit functionality immunity with gate oxide BD.
TUESDAY AFTERNOON
April 12, 2011

Session 2B: Circuit Reliability
Chair: Vijay Reddy, Texas Instruments
Co-Chair: Chris Kim, University of Minnesota

1:30 pm
Session Introduction

1:35 p.m.
2B-1 In Situ Screening Techniques for Defective Oxides in Devices for Automotive Applications (Invited), V. Malandrudcocolo, M. Ciappa, W. Fichtner, H. Rothleitner*, Institute of Technology (ETH), *Infineon Technologies

2:00 pm.

An on-chip 45nm test platform that directly monitors circuit performance degradation during dynamic operation is demonstrated. In contrast to traditional ring-oscillator (RO) based frequency measurements, it utilizes a Time-to-Digital Converter (TDC) with 2ps resolution to efficiently monitor circuit delay change on-the-fly. This new technique allows the capability of measuring signal edge degradation under various realistic circuit operating scenarios, such as asymmetric aging, dynamic voltage/frequency scaling, dynamic duty cycle factors, and temperature variations.

2:25 p.m.

A fast BTI characterization setup is introduced to study the Static Noise Margin (SNM) of cross-coupled inverters using metal gate / high-k devices. It is shown that static stress leads to significant SNM degradation due to PBTI at high stress voltage consistent with device level data. For dynamic stress the degradation becomes symmetric which can mask the degradation depending on the cell symmetry.

2:50 p.m.

Ring oscillator (RO) structures that separate NBTI and PBTI effects are implemented in a high-k metal gate technology. The measurement results clearly show significant RO frequency degradation from PBTI as well as NBTI. For comparison, RO structures with the same principle are also implemented in a SiO2/poly-gate technology, where PBTI is negligible. Experimental results show noticeable frequency degradation under NBTI-only stress mode but negligible degradation under PBTI-only mode, which illustrates the validity of the proposed principle and structures.

3:40 p.m.

In this paper we have developed a model to obtain drain current (ID) degradation at all transistor operating modes (linear, saturation and sub-threshold) during NBTI stress based on threshold voltage (VT) and mobility (\(\mu\)) degradation. This model provides a compact way to comprehend NBTI induced drain current degradation for transistors subject to multiple operating modes (e.g., dynamic voltage scaling, active/standby modes).
We develop a new universal smart test-structure solving the typical restrictions of BTI device array investigations. Our integrated structure combined with an adapted measurement methodology ensures very short and most notably uniform recovery times for each device of the entire array. This is the absolutely required precondition for statistical evaluations of the BTI degradation and recovery behavior.

Session 2C: Fabless and Product Reliability
Chair: Tom Anderson, Medtronic Inc.

10:35 a.m.
2C-2 Backend Low-k TDDDB Chip Reliability Simulator, M. Bashir, D.H. Kim, K. Athikulwongse, S.K. Lim and L. Milor, Georgia Institute of Technology

We present results from a simulator that evaluates low-k TDDDB chip lifetime from layout features. We present a model, the basis of our simulator, that links critical layout features to chip lifetimes. We use results from our simulator to study the effect of different layout optimizations on chip lifetime.

11:00 a.m.
2C-3 Determination of CPU Use Conditions, R. Kwasnick, A. Papathanasiou, M. Reilly, A. Rashid, B. Zaknoon and J. Falk, Intel Corporation

A requirement for knowledge-based qualification of IC’s is use condition inputs to physics-of-failure models. We present a methodology, applied to CPUs, which combines user surveys for on time and active time, and lab-based studies for time in performance states. We discuss the results and implications for knowledge-based qualification.

11:25 a.m.
2C-4 Si₃N₄ Extrinsic Defects and Capacitor Reliability, J. Scarpulla, E. King and J. Osborn, The Aerospace Corporation

The MIMCAPs seem to drive the reliability of MMICs in many cases, rather than the active devices themselves. We have examined MMIC extrinsic defect density by extracting it from test data available in the literature. We have noted that the extrinsic densities are surprisingly poor for thinner nitrides, and have proposed a simple model and some design charts for MMIC extrinsic reliability.

Session 2D: Memory
Chair: Sanjay Rangan, Intel
Co-Chair, Susumu Shuto, Toshiba

1:35 p.m.
2D-1 AC-DC Factor Sensitivity for DRAM Components Lifetime under Hot-Carrier Injection, S. Baeg, H. Nam, P. Chia*, S. Wen* and R. Wong*, Hanyang University at ERICA Campus, *Cisco Systems Inc.

Estimating operating lifetime is critical for dynamic random access memory (DRAM) components with hot-carrier injection (HCI). Using DC device life time to substitute a component life time can be too pessimistic and can disqualify good DRAM products. This work proposes the DC to AC lifetime ratio factor for DRAM components lifetime evaluation and its sensitivity over three parameters: device degradation, effective pumped voltage, and access frequency. The results are discussed with the measured substrate current for three representative DRAM technologies and correlated with component test data.

2:00 p.m.


The effect of mechanical stress induced by shallow trench isolation (STI) slope on the data retention characteristics of DRAM is investigated and a new electrical parameter for monitoring the mechanical stress is proposed. To maintain high and uniform retention time for the reliable operation of DRAM, the STI slope should not be vertical and should be kept below 86-degree. The new electrical parameter measures the current gain of the parasitic BJT in DRAM cell and shows a strong correlation with the retention time induced by the mechanical stress.

2:25 p.m.

2D-3 Hot Hole Induced Damage in 1T-FBRAM on Bulk FinFET, M. Aoulaiche, N. Collaert, A. Mercha, M. Rakowski, B. De Wachter, G. Groeseneken, L. Altin, M. Jurczak and Z. Lu*, Imec, *University of Florida

The reliability of one Transistor Floating Body -RAM bulk FinFET cell using BJT programming is investigated. It is shown that hot holes generated by impact ionization to write-1 degrade the cell endurance. Moreover, this degradation is increasing for shorter channel devices, which limits the cell scalability.

2:50 p.m.

2D-4 Effects of BTI during AHTOL on SRAM VMIN, S.-M. Lim, H. Hong, S. Yu1, M. Zhang, J. Park, Y. Kim, Samsung Electronics

It has been reported that change in SRAM VMIN during accelerated high temperature operating life (AHTOL) stress test is governed by Bias Temperature Instability (BTI) degradation on PD and PU transistors. However, PG transistor BTI at a practical duty ratio can alter SRAM VMIN shift during AHTOL appreciably. In this work, we have expanded SRAM VMIN shift investigation on the basis of PG BTI as well as PD and PU BTIs.

Session 2E: Thin Film Transistor
Chair: Andrea Cester, University of Padua

10:10 a.m.

2E-1 Flexible Biomedical Devices for Mapping Cardiac and Neural Electrophysiology (Invited), D.-H. Kim, J. Rogers, J. Viventi*, B. Litt*, University of Illinois at Urbana-Champaign, *University of Pennsylvania

10:35 a.m.


We subjected organic thin film transistors with different gate dielectrics to low-energy UV and visible light irradiation. Visible light induces only transient effects on the electrical characteristics, and a recovery takes place within 15 days. Similarly, UV light induces transient effects on devices with silicon nanoparticles at the pentacene/gate dielectric
interface. However, strong and permanent degradation is induced by UV irradiation on devices with HMDS-treated SiO2 gate dielectric.

11:00 a.m.

2E-3 A New Method for Predicting the Lifetime of Highly Stable Amorphous-Silicon Thin-Film Transistors From Accelerated Tests, T. Liu, S. Wagner and J. Sturm, Princeton University

We demonstrate a new method for predicting the lifetime of highly stable a-Si TFTs from accelerated tests, which is based on the stretched hyperbola fit for defect creation in a-Si. The rate of current drop can be accelerated by a factor of nearly 10,000 when the test temperature is raised to 160°C. This method will enable engineers to predict the stability and lifetime of a-Si TFTs in AMOLED displays with much greater confidence than in the past.

11:25 a.m.


We have investigated thin film transistors (TFTs) with ultra-thin polycrystalline silicon (poly-Si) of 77 Å - 185 Å. The TFT transfer characteristics such as ON current and effective mobility are dominated not by the thickness itself but by the grain size of poly-Si channel. When the poly-Si channel thickness is decreased with the same grain size, the sub-threshold TFT characteristics are improved without degradation of ON current and reliability properties. These results give us appropriate criteria to establish an excellent poly-Si channel in vertical NAND flash memory.
In this paper, we present the results of voltage-ramp dielectric breakdown and time-dependent dielectric breakdown experiments for contact–polysilicon control gate (CA/PC) intralevel dielectric stacks. Lifetime and its area scaling are discussed statistically with analysis of the global and local deviations using the electrical method. Optimized process reliability is evaluated by a test that measures the early life failure rate.

3:40 p.m.

**2F-5 Reliability Limitations to the Scaling of Porous Low-K Dielectrics**, S.-C. Lee, A. S. Oates, TSMC

We show that processes used to fabricate advanced porous dielectrics can exhibit reliability close to the intrinsic capability of the material. Combining this with simulations of failure distributions as a function of porosity and line edge roughness we demonstrate that failure times due to electrical breakdown rapidly decrease below k=2.3. Continued scaling will require greater understanding of the circuit impact of breakdown as well as materials innovations to improve robustness.

4:05 p.m.


The failure ratio of the three typical TDDB failure modes, including top interface, sidewall and bottom corner, has been identified for a direct polishing ULK/Cu BEOL structure at 40nm node. Evaluating a post-Cu CMP cleaning chemical with smooth Cu surface roughness; developing a stronger adhesion with multi-layer capping layer; using a little bit higher dielectric constant ULK; replacing a conventional pure Cu with a aluminum-doped Cu seed layer and optimizing the Cu barrier deposition with re-sputter processes can effectively extend the TDDB performance over three orders (>10000 years) in this study.

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**Session 2G: Extreme Environments**

Chair: Mark White, NASA

3:40 p.m.

**2G-1 Space Radiation Effects and Reliability Considerations for the Proposed Jupiter Europa Orbiter**, A. Johnston, California Institute of Technology

4:05 p.m.


We report for the first time reliability performance of non-volatile memory arrays based on Nanomech™ technology. The Nanomech™ non-volatile switch is able to maintain a programmed bit state across harsh environmental conditions, making this technology suitable for applications where traditional non-volatile memories fail.

4:30 p.m.

We use microanalysis to illustrate microstructure's effects on tin-whisker growth, explaining why large-grained and thin platings grow fewer whiskers, and Ni barriers and Sn-3%-Pb solder may not prevent whisker growth. We quantitatively predict the time-evolution of whisker length distributions, and develop a tin-whisker risk assessment framework from a materials perspective.