TUESDAY MORNING
June 3, 2014

General Session
Monarchy Room

Welcome Remarks
General Chair: Prasad Chaparala, Amazon Lab126

Introduction to Technical Program

Keynote Address 1
“Connecting the Dots to Achieve High Reliability and Quality”, Raj N. Master, Microsoft

Abstract
The ubiquitous trend towards a connected, digital, always-ON lifestyle is driving the development of electronic devices that have smaller form factors, higher performance requirements, along with expectations of reliability and quality. Consumers don’t buy products because of high quality but expect it. The result is a constant upward pressure on delivering high reliability at silicon, package and system level. Although this general trend holds for applications in the computing arena, gaming console arena, consumer electronics arena as well as in the portable electronics arena, the relative constraints on the cost, size and complexity of the products make this a challenging task. This is further made more difficult by unpredictable ways consumers may use the product. Microsoft evolution of hardware and reliability challenges of Surface will be described to achieve a highly reliable and quality product.

Biography
Raj joined Microsoft in 2008. He is General Manager for IC Packaging, Silicon Operations, Quality and Reliability for all hardware products in Microsoft. These include Xbox, Kinect, Surface, Accessories, Zune, Keyboard, Mouse, Webcam, and Roundtable etc.

Raj was Corporate Fellow and Chief Technologistist for AMD from 1996 - 2008. He was responsible to successfully transfer the IBM C4 / BGA technologies to AMD and set up high volume manufacturing in Penang which has to date produced more than 400 million flip chip assemblies. He led the Organic packaging development and manufacturing which is now in high volume production. As a part of that development he was responsible to select and develop package, component and material suppliers in USA to support high volume production. He is also responsible to build, qualify and provide technical direction to AMD Flip Chip Bumping and probing operations in Dresden, Germany. He led the selection and qualification of Unitive and bumping foundry and Amkor and ASE as assembly and test foundries. He provides technical guidance for equipment and processes for C4/BGA manufacturing lines in Suzhou, Penang and Singapore. He also provides technical expertise and guidance to product lines, Failure analysis, and reliability and quality organizations within AMD. He manages advanced packaging group involved in developing strategic enabling technologies. He was also manager of the Lead Free program of AMD working with US companies, Chinese Governments and EU to align the Lead Free exemptions.

Raj joined AMD after spending 21 years at IBM. He was Senior Technical Staff member at IBM prior to joining AMD. He was responsible for packaging development and manufacturing as related to C4, Ball Grid Array, Column Grid Array, Board Level Reliability and Multi Layer Ceramic Substrate.

Raj has 51 U.S. patents issued to him and has published over 80 technical papers.
Keynote Address 2
“Future of Mobile Computing”, Charles Bergan, Vice President of Engineering, Qualcomm, Inc.

Biography
Charles leads the software department for Qualcomm Research. Qualcomm Research invents breakthrough technologies that enhance Qualcomm’s portfolio of market-leading wireless products. While at Qualcomm, he has been involved in the research and development of CDMA, UMTS, UMB and LTE. Previously, he led the software development team at Ensemble Communications, a start-up company which was one of the leading developers of LMDS point-to-multipoint wireless backhaul systems. Charles has a B.S. in Computer Engineering, and an M.S. in Computer Science, both from the University of California, San Diego.

10:15 a.m.
Break

Session 2A - Interconnect Metalization Reliability

Session Co-Chairs: Cathryn J. Christiansen, IBM, Howard Gan, SMIC
Kings Ballroom

10:35 a.m.
Session Introduction

10:40 a.m.

Advanced technology nodes such as 32nm to 14nm often rely on a doped seed to reduce or eliminate Cu stress migration. However, this study shows that although Mn doping did improve SM, it was not enough to reduce the number of stress migration failures in sensitive "nose" structures to zero. Instead the via liner process was the key, with a contributing factor of wait time between Cu CMP and dielectric capping.

11:05 a.m.
2A.2 On The Distribution of Stress-Induced Voiding Failures Under Vias, G. Hall and D. Allman, ON Semiconductor

A physics-of-failure model for SIV for vias contacting wide metal leads is proposed. This model is used to fit long-term data from a 130 nm Cu/low-k BEOL process. Scaling forms are derived an Monte Carlo simulations are performed, showing use of seperate Weibull distributions for early and intermediate failures, or a single distribution dependent on the choice of void growth model. The presence of early transient statistics emphasize sample size and HTS readout strategy.

11:30 a.m.
2A.3 Lifetime Prediction of Stress-induced Voiding in Nose-Shape Lines by using a Stress-Diffusion Analytical Model, S. Yokogawa, Polytechnic University
Lifetime prediction model of SIV in Cu/low-k interconnects is proposed for the extrusion lines. Stress status of the base and extrusion lines is described by the Gompertz function. Stress-induced Cu ionic diffusion is formulated as a differential equation. Calculated lifetime as a solution of the differential equation is discussed compared to reported lifetime data. These results will provide valuable information about an actual layout design.

11:55 a.m.
2A.4

We studied EM performance of strapped Al layers with large dimension for lateral power device applications and found three unique failure modes: early, late, and no failure. We found severe M1 thickening that causes ILD and PO cracking. In certain samples, the PO holds the stress from the M1 thickening, resulting in compressive stress in M2 and thus immortality. The fatal failure mode is found to be the EM voiding at M2 steps.

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**Session 2B - Soft Errors**

Session Co-Chairs: Ethan Cannon, Boeing, Norbert Seifert, Intel
Kohala Ballroom 1-2

10:35 a.m.
Session Introduction

10:40 a.m.
2B.1
*Cross-Layer System Resilience at Affordable Power (Invited),* M.S. Gupta, J.A. Rivers, L. Wang, P. Bose, IBM T.J. Watson Research Center

In this paper, we address the challenge of achieving very high energy efficiency, while meeting target levels of performance and resilience to transient errors. We focus mainly at the processor chip level, while keeping in mind two ends of the system spectrum: (a) low power, real-time constrained embedded systems; and (b) extreme-scale high performance systems (or supercomputers). We advocate and illustrate the use of crosslayer resilience optimization as a general solution strategy.

11:05 a.m.
2B.2

Experiments performed at the Rutherford Appleton ISIS facility demonstrate the bias dependence of muon-induced single event upsets in delidded 28 nm static random access memories. Increased probability for upset is observed for memories operating at reduced voltages. Fully packaged parts are shown to be suitable to screen for low-energy muon sensitivity.

11:30 a.m.
2B.3

We experimentally show for the first time that radiation-induced upsets in PCM cells can occur when heavy ions strike a cell at an angle along the word line, due to amorphization of the heater-GST interface. The minimum LET required to produce this effect is larger than 12.5 MeV•mg-1•cm2, consistent with the lack of effects with atmospheric neutrons.

11:55 a.m.

2B.4

We report the correlation between natural boron (B10) and thermal neutron SER in advanced 28nm high-k/metal gate (HK/MG) technology node. Thermal neutron induced single event upset (SEU) depends on the concentration of B10 in the contact process adopted for boosting SRAM performance. Finally, the optimization of contact and eSiGe process can provide robust technology development against thermal and high energy neutron SER.

Session 2C - Compound/Opto Electronics

Session Co-Chairs: Eric Heller, AFRL, Jose Jimenez, Triquint Semiconductor
Kohala Ballroom 4

10:35 a.m.
Session Introduction

10:40 a.m.

2C.1
Toward a Physical Understanding of the Reliability-Limiting Ec-0.57 eV Trap in GaN HEMTs, A. Sasikumar, D. Cardwell, A. Arehart, J. Lu*, S. Kaun*, S. Keller*, U. Mishra*, J. Speck*, J. Pelz and S. Ringel, Ohio State University, *University of California, Santa Barbara

Recent reliability campaigns on AlGaN/GaN HEMTs have consistently revealed a critical Ec-0.57 eV trap that is responsible for drain-lag, RF output power degradation, and current-collapse. In this work, a comprehensive set of data obtained from a range of measurements and specialized test structures are combined and presented to reveal compelling evidence that this almost ubiquitous degradation-related defect is physically located in the GaN buffer thereby enabling opportunities for its correct identification, predictive-modeling, and possible removal/mitigation.

11:05 a.m.

2C.2

A method for extracting DIT profiles from subthreshold I-V characteristics is used to analyze data on a SiC MOSFET stressed for thirty minutes at 175°C with a gate bias of -20 V. Without knowing the
channel doping, the change in \( D_{IT} \) can be calculated when referenced to an energy level correlated with the threshold voltage.

11:30 a.m.
2C.3

A New Method for Extracting Interface State and Border Trap Densities in High-k/III-V MOSFETs, G. Sereni, L. Vandelli, L. Larcher, L. Morassi, D. Veksler* and G. Bersuker*, University of Modena and Reggio Emilia, *SEMATECH

In this study, we developed a new method for the extraction of interface traps and border traps. This method allows the determination of the real oxide capacitance value and to account separately for the effects caused by the response of the inversion layer (i.e. generation and recombination in the substrate) and trapping/emission by border and interface traps.

11:55 a.m.
2C.4

Modeling the Threshold Voltage Instability in SiC MOSFETs at High Operating Temperature, T. Kikuchi and M. Ciappa*, Toshiba Corporation, *ETH Zurich

The threshold voltage instability is a main reliability issue in Silicon Carbide MOS transistors submitted to gate bias stress. A new transient and temperature-dependent TCAD model based on phonon-assisted tunneling is proposed. The results are compared with a previously developed temperature-independent model and with experimental data.

Panel
12:00 p.m. Tuesday, June 3
Monarchy Room

TUESDAY AFTERNOON
June 3, 2014

Session 2D- Circuits Aging Simulation/Circuits Reliability

Session Chairs: Keith Green, Texas Instruments, Yu Cao, ASU
Kings Ballroom

2:20 p.m.
Session Introduction

2:25 p.m.
2D.1

Mixed-voltage I/O interfaces must be designed to overcome several problems, such as TDDDB and HCI degradation. This paper proposes for the first time to demonstrate a complete design optimization flow for reliability including both architectural changes and automated sizing procedure and tool.

2:50 p.m.
2D.2

For the first time, the frequency fluctuation effect in a fast DVFS environment was analyzed with a proposed empirical BTI stress-relaxation model based on the superposition property. Based on the actual VDD and operating frequency information collected from an ARM Cortex A15 processor based Android system, the proposed modeling method is readily applied to study the fast frequency shift transients under different benchmark applications.

3:15 p.m.
2D.3

Positive feedback between bias current and channel hot carrier causes enhanced degradation rate in diode-connected devices, referred as Bias Runaway. Based on 65nm silicon data, this paper investigates the critical condition that triggers bias runaway, and the impact of gate length tuning. Develop compact models and the simulation methodology for circuit diagnosis, and proposes design solutions and the trade-offs to avoid bias runaway. It Identifies stability issues for such feedback systems for reliable AMS designs.

3:40 p.m.
2D.4

Manufacturers frequently aim to maximize the performance of their CMOS applications by various means, notably by increasing Vcc of critical sub-circuits. This, however, typically occurs at the expense of the application reliability. Specifically, serially connected nFET transistors are apparently vulnerable to PBTI. We employ CET maps and TDDS to describe DC and AC PBTI mean and distribution behavior and we demonstrate net performance gain at no PBTI penalty. Maximum Vcc of is limited by HBD.

4:05 p.m.
2D.5
New Insights about Oxide Breakdown Occurrence at Circuit Level, M. Saliva, F. Cacho, V. Huard, D. Angot, X. Federspiel, M. Durand, M. Parra, A. Bravaix* and L. Anghel**, STMicroelectronics, *IM2NP-ISEN, **TIMA

Lifetime extension based on device level parameters drift is difficult to handle, an accurate BD model is thus mandatory for predictive simulation at circuit level. For the first time, a dedicated digital circuit has been designed to track multiple BD events. This circuit (called Flipper) has been used to enhance BD of custom cells. Measurements of BD time, delay and Iddq are compared with BD results obtained at device level to simulation.

4:30 p.m.
2D.6
Isolated/combined NMOS and PMOS contributions to frequency shift and device degradation distribution in a RO are characterized. Qualitative model is proposed to explain the nonlinearity of frequency shift. Distinct disagreements appear if discrete device DC model applied to RO simulation. DVT extracted at RO operating frequency at 50 percentile can make HSPICE aging model more precise. RO itself should be a standard reliability test structure to bridge the gap to fast switching logic circuits.

Session 2E – Memory

Session Co-Chairs: Alessandro Spinelli, University of Polimi, Shosuke Fujii, Toshiba
Kohala Ballroom 1-2

2:20 p.m.
Session Introduction

2:25 p.m.
2E.1

Numerous scaling limitations of NAND flash memory have arisen due to the intrinsic nature of the operational principle of NAND flash memory and those limitations eventually lead to a paradigm shift in the NAND flash technology from the planar cell to the vertical NAND cell. In this paper, the limitations of scaling which induce the evolution of the NAND cell as well as the current trends of NAND technology are reviewed.

2:50 p.m.
2E.2

We present a semi-analytical model for charge trapping and detrapping in NAND Flash memories, accounting for all the main physical aspects of the phenomenon: charge discreteness, spectral distribution of detrapping time constants, statistical charge capture and emission. The model provides the entire D VT distribution after cycling and bake without any need to resort to lengthy Monte Carlo simulations. It is then a powerful tool for the predictive analysis of cycling-induced threshold-voltage instabilities.

3:15 p.m.
2E.3

Scaling of floating gate NAND Flash will require switching from conventional control gate wrap-around cells to fully planar memory cells with HFG and high-κ IGD stacks. High density of electron trapping in these IGD materials remains a major concern. Furthermore, there is a lack of measurement methods to separate IGD charging/discharging from FG charging/discharging. In this work a fast response technique is developed to characterize the HFG/IGD interface

3:40 p.m.
2E.4
Study on the Vt Variation and Bias Temperature Instability Characteristics of TiN/W and TiN Metal Buried-Gate Transistor in DRAM Application, T.-S. Jang, K.-D. Kim, M.-S. Yoo, Y.-T. Kim, S.-Y. Cha, J.-G. Jeong and S.-H. Lee, SK Hynix Inc.

A metal gate electrode is necessary for the application of buried-gate (BG) cell transistor in DRAM. In this study, the Vt variation and positive bias temperature instability (PBTI) of TiN/W and TiN metal BG cell transistors are characterized. Also, the mechanism for different electrical properties between these two metal gates is discussed.

4:05 p.m.
2E.5
NaMLab gGmbH, *Fraunhofer Center Nanoelectronic Technologies, **GLOBALFOUNDRIES

The scope of this paper is to clarify the origin of the endurance degradation in HfO2-based non-volatile ferroelectric field effect transistors. Several possible degradation mechanisms are proposed and verified. The limited endurance properties were found to be linked to the transistor gate stack rather than to the ferroelectric material itself. Based on the gate leakage current measurements and the trapping analyses the degradation of the interfacial layer was identified as the main degradation mechanism.

4:30 p.m.
2E.6

A back-end integrated Resistive Random Access Memory (ReRAM) (TiN/HfO2/Ti/TiN) in advanced 28nm CMOS process is evaluated. Significant operating margins and high performances identified at device level (read margin, low power set/reset, endurance and retention) are demonstrated to be significantly reduced on larger statistics, i.e. characterized within 1kbit arrays. The High Resistance State (HRS) dispersion, identified as a limiting factor, is modeled through the “tunneling barrier thickness” variation. The optimization through electrical condition tuning is discussed. A global overview of HfO2 material performances is assessed on statistical basis and projection for larger array integration is discussed.

Session 2F - Chip Package Interaction

Session Co-Chairs: Kristof Croes, IMEC, Alan Lucero, Intel
Kohala Ballroom 4

2:20 p.m.
Session Introduction

2:25 PM
2F.1
Package Reliability and Performance Trends in an Era of Product Integration (Invited), J. He, Intel Corporation
Product differentiation is expected to accelerate and will encompass integration of product functionality into single and multiple die on package as well as multiple die/packages on board. Novel packaging designs will lead to incorporation of new materials and processes from which a comprehensive understanding of operating conditions at system and subcomponent level will be required to ensure reliability at minimum impact to cost & performance. Reliability tests, models and analysis must evolve to encompass emerging failure mechanisms and geometric effects not considered when standards were originally authored. This manuscript will show trends in packaging and materials along with examples of emerging failure mechanisms that need to be understood to ensure reliability in highly integrated products.

2:50 p.m.

2F.2
Mechanical Stability of Cu/low-k BEOL Interconnects, M. Gonzalez, K. Vansreels, V. Cherman, K. Croes, L. Kljucar, I. De Wolf and Z. Tőkei, imec

Different approaches combining Finite Element Simulations and in-situ electrical measurement during a BABSI test are proven to be ideal combination to quantitative compare the strength of BEOL layers. It is shown that detectable mechanical failures during BABSI test are insufficient to detect early opens of the metal interconnections. A good agreement was found between the applied loads to the BEOL stack, the response of stress sensors below the Cu pillar and finite element simulations.

3:15 p.m.

2F.3

In a summary, this is the first time a systematic study was performed using both simulation and experiment to understand the effects of various assembly and reliability stresses on CPI effects of an actual ASIC product. The results are very helpful to better understand where and when the worst case CPI stress occurs so the package designer and assembler can use this information to mitigate the CPI induced failures and assess the reliability risks and predict lifetime.

3:40 p.m.

2F.4

IC components experience temperature and power cycles during operation in end use environments. A complete assessment of the cumulative number of temperature cycles and extremes from shipping/storage and through end-customer use is required to guarantee product performance and reliability. This paper will use data to develop acceleration models for observed failure modes. These models will be used in conjunction with known use conditions to estimate lifetime requirements. These requirements will be compared to JEDEC standards.

4:05 p.m.

2F.5
A Fabless Company’s Perspective on Large Die Chip Package Interaction (CPI) Challenges (Invited), K. Chanda and V. Mahadev, Altera Corporation

FPGAs continue to evolve at most advanced semiconductor technology nodes, and in larger die and package form factors to meet the increasing demands for performance from high end systems. Scaling of
the low-k dielectric material in the die at these nodes poses a challenge, not only for process integration, but also for Chip Package Interaction (CPI) reliability. Here we review some of the major concerns with large die CPI reliability in light of this relentless march towards lower-k material. We also propose a need for collaboration across multiple parties (Fab, Component Supplier, Assembly House, Board Supplier, System Designer, and End Customer) in order to successfully meet performance goals without sacrificing reliability needs for the system.

WEDNESDAY MORNING
June 4, 2014

Session 3A - BEOL Dielectric Reliability

Session Co-Chairs: Oliver Aubel, GlobalFoundries, Fen Chen, IBM
Kings Ballroom

8:00 a.m.
Session Introduction

8:05 a.m.


Both MOL PC-CA spacer dielectric and BEOL low-k dielectric breakdown data are commonly convoluted with multiple variables present in the data. In this paper, a new big data generation method plus a new data deconvolution procedure is proposed to soundly evaluate both MOL and BEOL dielectric Vbd/TDDB data. A new process and reliability quality index, die-to-die variation distribution, is for the first time quantitatively established for process diagnostics and more accurate reliability failure rate determination.

8:30 a.m.

3A.2 Towards the Understanding of Intrinsic Degradation and Breakdown Mechanisms of a SiOCH Low-k Dielectric, C. Wu*, Y. Li, Y. Barbarin, I. Ciofi, B. Tang*, T. Kauerauf, K. Croes, J. Bömmels, I. De Wolf* and Z. Tőkei, IMEC, *also with KU Leuven

The degradation and breakdown mechanisms of a SiOCH low-k material with k=2.3 (25% porosity) and thicknesses ranging from 90nm to 20nm were investigated. The dielectric failure is proven to be intrinsic. It is shown that stress induced leakage current can be used as a measure of dielectric degradation. Based on our experimental results, it is suggested that the impact damage model has a better accuracy for low field lifetime prediction.

8:55 a.m.

3A.3 A New Methodology For Copper/Low-K Dielectric Reliability Prediction, S.-C. Lee and A.S. Oates, TSMC

We investigate Cu interconnect geometric variability impact on low-k dielectric reliability. We propose a new methodology to de-convolute the intrinsic low-k material and interconnect geometric components
from acceleration testing failure data, which allows a straightforward prediction of low-k failure time distributions at use conditions. Our analysis shows that geometric variability impact on low-k dielectric reliability depends strongly on the lithography patterning technique.

9:20 a.m.

3A.4

**Study on Vertical TDDB Degradation Mechanism and its Relation to Lateral TDDB in Cu/Low-k Damascene Structures**, N. Suzumura, M. Ogasawara, T. Furuhashi and T. Koyama, Renesas Electronics Corporation

We investigated the VTDDDB (inter-level metals) degradation mechanism in Cu/low-k damascene structures and discussed its relation to LTDDDB (intra-level metals). It was found that the VTDDDB might become a reliability issue for high voltage operation devices. And VTDDDB is limited by the intrinsic breakdown of the ILD film in the Via region. And the VTDDDB failure mechanism is associated with the LTDDDB failure mechanism at high temperature from the temperature and electric-field characteristics.

9:45 a.m.

3A.5


Recent research indicate that Cu plays an significant role in the TDDB break down mechanism. In this work, we used a direct experimental examination on the underlying physics and assumptions of the model and demonstrated the excellent agreement between our experiment results and the physics picture on Cu ion assisted interfacial Cu diffusion model proposed by F. Chen et al, and also a better methodology for intrinsic $\beta$ extraction.

**Session 3B - Product IC Reliability**

Session Co-Chairs: Sangwoo Pae, Samsung, You Wen Yau, Qualcomm
Kohala Ballroom 1-2

8:00 a.m.

Session Introduction

8:05 a.m.

3B.1


This paper showcases universality of NBTI parameters (time, bias, temperature, AC frequency and duty cycle) across different industries and technology nodes. Strong correlation between device and circuit/product NBTI has been established. Different aspects of small area device variability are discussed. Features that are important from an industrial perspective are highlighted, and any NBTI model should address these aspects to be considered relevant.

8:30 a.m.

3B.2

**Mission Profiles Derived from Lifetests and Field Return Data Using Inverse Problem Theory**, Z. Liang and R.M. Kho, NXP Semiconductors
The use conditions as described in Mission Profiles are key to set reliability requirements. This paper describes a method of Mission Profile deduction from reliability stresses and field return data, using the inverse problem theory. This method has been applied to two cases. These new insights can be used for more accurate failure rate prediction in the field and lead to more reliable risk assessment.

8:55 a.m.

3B.3
**Voltage Ramp Stress Test to Determine TDDB Performance in SRAM Vehicle, J.-G. Ahn, S. Parameswaran, D. Tsaggaris, C.-W. Ku, P.-C. Yeh and J. Chang, Xilinx, Inc.**

We applied Voltage Ramp Stress Test (VRST) to an SRAM test vehicle and compared the obtained Vfail distribution with theoretical predictions from various TDDB failure criteria. Measured Vfail results are matched with the prediction from TDDB failure criterion of Ig/Ig0=1000 or more. In order to estimate effective gate current increase, we developed a numerical method to predict effective Igate with TDDB stress. It was applied to VRST condition and shows good agreement with measured data.

9:20 a.m.

3B.4
**Systematic Reliability Characterizations on Average Output Voltage (AVO) Shift of Display Driver IC by HTOL, J. Kim, D. Kim, M. Choe, K. Bae, S. Shin, S. Pae and J. Park, Samsung Electronics Co., Ltd.**

HTOL study on Display Driver IC using 70nm process technology is presented in this work. DDI is an IC that controls the display color pixels. The Average Output Voltage (AVO) and Deviation Output Voltage (DVO) are two key critical parameters for reliability that determines the quality of display. We report the fails seen in early product HTOL testing due to Vt mismatches of amplifier transistor after aging and fixes implemented to significantly improve product reliability.

9:45 a.m.

3B.5
**Impact of VLSI Scaling on Die Qualification, A. Haggag, M. Phillips and J.K.J. Lee*, Freescale Semiconductor, Inc., *Cisco**

As technology scales, the dominant product failure modes under voltage, temperature and humidity stress change to ones with higher acceleration factors suggesting standard product qualification guidelines of 1000hrs or 1000cycle stresses may be overly aggressive for predicting failure rate in the field. We show even for an aggressive mission profile typical qualification likely covers >10x mission life.

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**Session 3C - Process Integration**

Session Co-Chairs: Motoyuki Sato, Toshiba, Xavier Garros, CEA-LETI
Kohala Ballroom 4

8:00 a.m.
Session Introduction

8:05 AM

3C.1
Dark current is a major concern for the CMOS Image sensor. If the Shockley-Read-Hall generation creates this current, the origin of defects, this gives the blemish pixels. The interface states generate the mean dark current of the pixel. The good use of Forming Gas anneal is needed to passivate these interfaces. Next, all the plasma processes have to be optimized not to dissociate the passivation, because of the deep UV and the electric field created by plasma. Finally, some process improvements, or the choice of a p-type pixel with holes, collection, should give robust image sensors with low and controlled dark current.

8:30 a.m.
3C.2
SILC and Gate Oxide Breakdown Characterization of 22nm Tri-gate Technology, S. Ramey and J. Hicks, Intel Corp.

The SILC behavior in 22nm tri-gate devices is reduced compared to 32nm planar devices due to gate optimization and benefits from the tri-gate architecture. A product risk assessment method is presented indicating low risk from SILC. A full technology characterization is presented for NMOS, PMOS, stress voltage and polarity.

8:55 a.m.
3C.3
Aluminum Charge/Dipole Passivation Induced By Hydrogen Diffusion In High-K Metal Gate, G. Ribes, V. Barral*, S. Chhun, M. Gros-Jean, P. Caubet and D. Petit, STMicroelectronics, *LETI

In this work, it has been demonstrated that H species can suppress Al charge/dipole resulting in a Vth shift (140mV). Solutions to avoid this critical effect have been proposed. Indeed transferring oxygen vacancies from HK to IL results in the creation of Si-Si in IL. These defects known as neutral hydrogen traps capture a majority of hydrogen species. The diffusion of oxygen vacancies in IL stabilizes the HK stacks properties and suppresses the Vth shift.

9:20 a.m.
3C.4

CV-NBTI study on high-k first MOS capacitors with slant etched SiO2 indicated that the significant increase in NBTI at UT-EOT is triggered by EWF roll-off originating from the bottom interface of the gate stacks, probably the generation of positive Qfix in SiOx, which causes considerable offset Eox. In contrast, reduction of the offset Eox by introducing negative Qfix in SiOx or lowering the channel doping density were shown to be potential ways to reduce NBTI.

9:45 a.m.
3C.5

Positive bias stress in the InGaAs channel nMOSFETs with gate last Al2O3 and gate-first ZrO2/Al2O3 process flows is investigated. Threshold voltage shift ($\Delta V_T$) during stress is primarily caused by a
recoverable electron trapping at the pre-existing defects located predominantly in the Al2O3 interfacial layer (IL). Generation of new electron trapping defects is found to occur in the dielectric region adjacent to the substrate, while trap generation in the high-k bulk is negligible.

Break
10:10 a.m.

Session 3D - MEMS Sensor Reliability

Session Co-Chairs: Georgios Papaioannou, University of Athens, Michael Nicoladis, IMAG
Kings Ballroom

10:30 a.m.
Session Introduction

10:35 a.m.
3D.1 Double-Sampling Architectures (Invited), M. Nicolaidis, TIMA (CNRS, Genoble INP, UJF)

Aggressive technology scaling impacts dramatically parametric yield and reliability in advanced nanometric nodes, and can become showstoppers when moving deeper to the sub-10nm domain. To mitigate this issue various approaches have been proposed including increasing guard-bands, fault-tolerant design, and canary circuits. Each of these approaches have certain fundamental drawbacks such as: large performance penalty, and/or large area and power penalty, and/or false positives and false negatives, and/or insufficient coverage of the failure mechanisms encountered in the deep nanometric domain. This paper presents an approach able to mitigate all these failures at low area, power, and performance penalties.

11:00 a.m.
3D.2 Error-Resilient Design Techniques for Reliable and Dependable Computing (Invited), S. Das, D. Bull, and P. Whatmough, ARM Ltd.

11:25 a.m.

Resilient and adaptive circuit techniques enable architectures that are tolerant to static and dynamic variations such as process variation, voltage droops, temperature and aging. These circuit techniques are key to reduce voltage, temperature and reliability guardbands. Guardbands are used to guarantee that systems will operate correctly when subjected to the variations mentioned previously. However, they incur in significant loss in performance and energy efficiency that tax the system. In addition, these added guardbands also impact the reliability of the system. In this work we present resilient and adaptive circuit techniques implemented in microprocessor and graphics pipelines that demonstrate significant power, guardband reduction and energy efficiency and performance gain.

11:50 a.m.
3D.4 Reliability Issues in GaN and SiC Power Devices (Invited), T. Ueda, Panasonic Corporation
Session 3E - 3D/TSV Reliability

Session Co-Chairs: Steve Groothuis, Micron Technology, Sudarshan Rangaraj, Intel
Kohala Ballroom 1-2

10:30 a.m.
Session Introduction

10:35 a.m.
3E.1

TSV Cu pumping may result in deformations of the Cu/low-k interconnect wiring above the TSVs and affect the BEOL metal and dielectric reliability. In this paper, the impact of Cu TSVs on the BEOL reliability is investigated, including stress induced voiding of Cu vias and the low-k dielectric reliability in both inter- and intralevel configurations. Also, possible solutions to mitigate the reliability risks are discussed.

11:00 a.m.
3E.2
Mass Transport-Induced Failure in Direct Copper (Cu) Bonding Interconnects for 3-D Integration - The electromigration Point of View, S. Moreau, Y. Beilliard, P. Coudrain*, D. Bouchu, R. Taibi, and L. Di Cioccio, CEA, LETI, *STMicroelectronics

Even if 3-D integration is not yet an industrial reality, every company needs to demonstrate the reliability of its solutions. This paper focuses on an in depth study of direct Cu bonding interconnects resistance against the electromigration phenomenon. Black's parameters are extracted and show a higher EM reliability than standard interconnects (BEoL, TSV, etc.) thanks to a higher activation energy. In addition, these preliminary results seem to be influenced by the size of the bonding area.

11:25 a.m.
3E.3
Effects of Sidewall Scallops on Open Tungsten TSVs, L. Filipovic, R.L. de Oriio, S. Selberherr, A. Singulani*, F. Roger* and R. Minixhofer*, TU Wien, *ams AG

The processes required to generate several TSV geometries are simulated and the resulting geometry is imported into a finite element tool for parameter extraction and reliability analysis. The electrical models, which were proven against experimental measurements with non-scaled TSV geometries, are applied to the generated scalloped TSVs. The electrical parameters, thermo-mechanical stress, and electromigration induced stress for the structures are calculated and the variation in TSV performance, when the sidewall scallop size is varied, is analyzed.

11:50 a.m.
3E.4
The retention time of memory cell in 50-µm thick DRAM chip (CMP-treated) dramatically degraded after intentional Cu diffusion from the backside surface at 300°C. Meanwhile, the retention time of DRAM cell in the DRAM chip (DP-treated) not degraded. The retention time of some memory cells, which were departed 20–50-µm from Cu TSV array, were began to degrade after annealing at 300°C as the blocking property of some sputtered-Ta barrier layers in TSV array not enough.

**Session 3F - Failure Analysis**

Session Co-Chairs: Ed Cole, Sandia National Labs, Shuichi Kudo, Renesas
Kohala Ballroom 4

*10:30 a.m.*
Session Introduction

*10:35 a.m.*

**3F.1**

**Fundamentals and Future Applications of Laser Voltage Probing**, U. Kindereit, Qualcomm Technologies, Inc.

This paper will give an overview of the history of Laser Voltage Probing – it will provide insight into various detection schemes and measurement methods that were and currently are used in the industry, explain details about the physical background of the signal generation process and discuss challenges for future technology nodes and highlight development areas.

*11:00 a.m.*

**3F.2**

**Backside Device Physical Analysis for Yield and Reliability of Advanced Bulk-Si CMOS ICs**, Y. Li and H. Marks, nVidia Corporation

This paper describes a backside defect localization and analysis methodology for effective identification of failures and weakness in advanced flip-chip packaged bulk-Si CMOS IC devices. Case studies demonstrate applications of the backside methodology for e-fuse reliability, in examination of fab Optical Proximity Correction (OPC) end-result and in isolating a yield limiting design issue in a MOM capacitor and a process issue with missing contacts.

*11:25 a.m.*

**3F.3**

**A Novel Analysis of Oxide Breakdown Based on Dynamic Observation using Ultra-High Speed Video Capturing Up to 10,000,000 Frames Per Second**, R. Kuroda, F. Shao, D. Kimoto, K. Furukawa, H. Sugo, T. Takeda, K. Miyachi, Y. Tochigi, A. Teramoto and S. Sugawa, Tohoku University

Real time observations of 100 nm-thick oxide breakdown realized by up to 10M fps ultra-high speed video capturing were demonstrated. The correlation of TDDB failure mode and light emission mode was confirmed. The capture and emission of a critical trap of a percolation as well as transitions of percolation paths were dynamically analyzed by the captured video. Real time observations of oxide breakdown event are useful for modeling and developing robust device structures and processes.

*11:50 a.m.*

**3F.4**

The limits of continuous-wave laser-assisted device alteration (LADA) make it difficult to isolate interaction sites to the transistor level on 28nm bulk silicon integrated circuits. Therefore, time-resolved LADA has an important timing advantage when the laser pulse arrives just prior to the critical time interaction window at a given transistor. By understanding how to use this timing relationship, picosecond timing waveforms have been obtained.

Workshops/Panel Discussion
12:15 p.m. – 2:15 p.m.

WEDNESDAY AFTERNOON
June 4, 2014

Session 4A - Transistor - Failure Analysis

Session Co-Chairs: James H. Stathis, IBM, Souvik Mahapatra, IIT Mumbai
Kings Ballroom

2:15 p.m.
Session Introduction

2:20 p.m.

4A.1 Modeling of Transient and Static Components of Intrinsic Emission from VLSI Circuits, A. Bahgat Shehata, F. Stellari, A. Weger and P. Song, IBM T.J. Watson Research Center

This work presents a study of the effect of electrical parameters, such as transistor threshold, supply voltage, signal frequency, and duty cycle, on the intensity of transient and static emission components in time-integrated images acquired from VLSI circuits. Time-integrated and Time-Resolved Emission data were acquired from a 32 nm SOI test-chip at different operating conditions to separate the transient and static components of circuit emission. A novel model to explain the experimental data is proposed.

2:45 p.m.


We study sub-threshold degradation in scaled NMOS transistors and propose a unified channel current ($I_S$) and drain-to-source voltage ($V_{DS}$) dependent lifetime model for a wide range of bias conditions. The lifetime dependence on VDS suggests that degradation is limited by the maximum energy available for the channel electron in short channel transistors.

3:10 p.m.

4A.3 Origin and Implication of Hot Carrier Degradation of Gate-all-around III-V MOSFETs, S.H. Shin, M. Wahab, M. Masuduzzaman, M. Si, J. Gu, P.D. Ye, M.A. Alam, Purdue University
We show that the HCI stress bias condition for the maximum damage is VGS~VDS for InGaAs GAA NW structure. Several experiments confirmed (ΔIOFF, ΔVth, and ΔSS) that electron trapping dominates HCI degradation. Finally, we verify HCI damage is on drain side by flipping current flows. Remarkably, despite the dramatic difference in materials/geometry, HCI in GAA-NW is essentially classical, suggesting that HCI-reliability may not be a bottleneck for the adoption of GAA-NW as a sub-20nm technology.

3:35 p.m.
4A.4

The impact of self-heating on device reliability characterization, such as BTI, HCI, and TDDB, is extensively examined in this work. Self-heating effect (SHE) and its impact on device level reliability mechanisms is studied, and an empirical model for layout dependent SHE is established. V_T shift is proposed for NBTI&HCI characterization index from SHE considerations. In HCI stress, V_g = 0.6~0.8Vd is suggested to meet the reasonable operation power and reduce self-heating induced temperature rising.

4:00 p.m.
4A.5

Based on a detailed analysis at the single defect level, we conclude that RTN and the recoverable component of NBTI are due to the same defects. This implies that conventional RTN and BTI must be characterized together for meaningful results. In particular, from an RTN perspective, these defects may become charged simultaneously by chance during the lifetime of the device, resulting in considerable shifts. Conversely, BTI will have a large stochastic contribution not captured by standard models, making extrapolation from stress to operating conditions more challenging.

4:25 p.m.
4A.6
**Analyzing Correlation Between Multiple Traps in RTN Characteristics**, T. Obara, A. Teramoto, A. Yonezawa, R. Kuroda, S. Sugawa, and T. Ohmi, Tohoku University

The three and four states RTN were analyzed from the 131,072 MOSFETs. There were two types RTN, firstly multiple traps are independent from each other, secondly the multiple traps have the correlation. In the 1st case we can apply the analysis method of two states RTN and in the 2nd case we have to consider the correlation between traps. These analyzing method help us to understand the RTN mechanism.

**Session 4B - Electronic Systems Reliability**

Session Co-Chairs: Amit Marathe, Microsoft, Ajay Kamath, Google
Kohala Ballroom 1-2

2:15 p.m.
Session Introduction

2:20 p.m.
4B.1

The Role of Hardware Security in Product Reliability (Invited), K. Bernstein

2:45 p.m.

4B.2

Simulation-Based Reliability Evaluation for Analog Applications, E. Weber and K. Echtle, University of Duisburg-Essen

In this paper we present a new technology to improve the efficiency of reliability evaluation for analog circuits based on fault simulation. A novel fault simulation tool has been developed and applied to reliability prediction. In traditional reliability prediction the evaluation consists of serial systems or explicit redundancy in the system structure. In this new approach we consider all types of redundancy, even hidden redundancy and fault tolerance.

3:10 p.m.

4B.3


The reliability/performance trade-off in SSDs has been simulated to estimate the impact of adaptive read algorithms adopted to extend the NAND flash lifetimes. Results also show that an accurate analysis requires the use of a different BER for each single NAND flash chip constituting the storage medium.

3:35 p.m.

4B.4


The SOFR model is modified for SOCs in consumer electronics applications such as game consoles for advanced logic technology nodes (~2X nm). Using a representative voltage/temperature dataset from XBOX ONE SOC operation, a quantitative measure of “degree of over-design coefficient (df)” is developed to better understand the impact of worst case reliability assumptions on thermal design. It is emphasized that use of SOFR model minimizes thermal over-design, thereby improving user experience, without compromising reliability.

4:00 p.m.

4B.5


An AVSI-sponsored project is developing a simple reliability estimation methodology for random failure rate and time to intrinsic wearout. Using similar PoF and statistical models for both, we seek data and analysis from semiconductor manufacturers, without proprietary details, and scale results between usage conditions. The driving concerns are common among high-reliability industries, so the methodology and desired semiconductor industry engagement have applicability beyond aerospace. This paper reviews motivation, methodology and prototype spreadsheet-based tool status.

4:25 p.m.
4B.6
Hard Disk Drive Failure Physics and the Reliability Process for Consumer Electronics Applications (Invited), B. Hiller

Session 4C - ESD and Latchup

Session Co-Chairs: Steven Voldman, Independent Consultant, Ming Dou Ker, National University of Taiwan
Kohala Ballroom 4

2:15 p.m.
Session Introduction

2:20 p.m.
4C.1
Novel Area-Efficient Technique for Improving ESD Performance of Drain Extended Transistors, A. Appaswamy, F. Farbiz and A. Salman, Texas Instruments

In this work, we demonstrate a highly area-efficient self-protection strategy for drain extended MOS devices using drain-side selective silicide blocking that improves the ESD area efficiency by more than 70% over current state-of-the-art solutions. Also, we report and provide physical understanding on the non-scaling breakdown behavior in isolated DEMOS devices. Finally, we show that drain side silicide blocking improves the robustness of isolated DEMOS devices as well.

2:45 p.m.
4C.2

Early failure has been observed during CDM ESD stress on high-voltage tolerant nLDMOS-SCR devices in a standard low-voltage CMOS technology due to the gate oxide (GOX) degradation. In this work, we propose a special p+/n+ differential doped gate which boosts the CDM ESD failure current level with a factor of 3 to 9. The in-depth physical study further indicates the improvement on off-state GOX reliability in the devices with the proposed differential doped gate.

3:10 p.m.
4C.3
Monolithic ESD Protection for Distributed High Speed Applications in 28-nm CMOS Technology, J. Salcedo, S. Parthasarathy and J.-J. Hajjar, Analog Devices, Inc.

A monolithic electrostatic discharge (ESD) input/output (IO) cell is introduced. This protection cell is demonstrated in a 28-nm high-k metal-gate CMOS technology. It is synthesized with distributed IO circuit components for in-situ protection in emerging high speed data rate signal processing systems-on-a-chip (SoCs). The protection cell rapidly activates complementary discharge paths during the different ESD stress modes at the IO, achieving target ESD robustness and low standing leakage (< 10 nA at 125 C).

3:35 p.m.
4C.4
An ESD supply clamp architecture that is tolerant to 5V power-supplies in 65nm CMOS is introduced. This architecture makes use of stacked NW capacitors and vertical NPN devices in its trigger network. This helps to simplify the triggering circuit and also improves the overall reliability of the clamp with a much lower leakage performance. The complimentary MOS output stage is chosen in order to improve the high voltage tolerance of the clamp while minimizing leakage.

4:00 p.m.

**4C.5**

*Novel Dual Direction PNP with Self-bias Ring Structure, T.-C. Tsai, J.-W. Lee, M.-F. Tsai, Y.-F. Chang, S.-M. Cheng and M.-H. Song, TSMC*

A novel trigger voltage and holding voltage tunable dual direction PNP with self-bias ring is proposed and demonstrated in this work to suppress leakage current with floating isolation ring structure. Through implementing the self-bias ring, not only latch-up(LU) immunity could be enhanced by more than 2.5X, but the leakage current level could be suppressed by more than 20X and so does the standby power consumption for ESD protection circuit.

**POSTER PRESENTATIONS**
**WEDNESDAY, June 4, 2014**

**6:00 p.m.**

**PS.BD1**

*Electrical Breakdown in Polymers for BEOL Applications: Dielectric Heating and Humidity Effects, S. Palit and M.A. Alam, Purdue University*

Polymer materials are used as low-k BEOL dielectrics in IC fabrication. Long term usage results in dielectric breakdown - a catastrophic loss of insulating properties. Additionally, polymer materials are susceptible to slow chemical degradation due to moisture, reducing their lifetimes under nominal electric fields. We develop numerical and analytical framework for dielectric breakdown, show that dielectric heating is the dominant degradation mechanism under AC stress, and study the effect of ambient humidity on lifetime.

**PS.BD2**


Reduced gate-to-contact thickness is prompting a search for compatible spacer dielectrics with reduced dielectric constants (κ). We compare the reliability of the traditional spacer dielectric, Si3N4, with a lower κ material, SiBCN. Weibull slopes and power-law exponent are measured to be close to SiO2. Guidance is given on the minimum SiBCN spacer thickness.

**PS.BD3**

*TDDDB At Low Voltages: An Electrochemical Perspective, R. Muralidhar, T. Shaw, F. Chen*, P. Oldiges**, D. Edelstein, S. Cohen, R. Achanta*, G. Bonilla, M. Bazant**, IBM Thomas J. Watson Research Center, *IBM Microelectronics, **Massachusetts Institute of Technology*

As we scale BEOL geometries, extrinsic wearout mechanisms involving copper and moisture can impact TDDB reliability while intrinsic high field mechanisms become less important. In this paper, we
investigate extrinsic reliability in low voltage regime where electro-chemical redox reactions are possible. We present analytic solution for limiting cases that show TDDB lifetime dependence on voltage or electric field dependence depending on relative rates of electrode reactions and field assisted ion transport.

**PS.BD4**  
**Low-Field TDDB Reliability Data to Enable Accurate Lifetime Predictions, E. Liniger, S. Cohen and G. Bonilla, IBM T.J. Watson Research Center**

A 30 month module-based low-field TDDB study on 90nm pitch Back End of the Line (BEOL) interconnect structures has shown that the commonly used root-E extrapolation model is overly conservative at predicting TDDB lifetimes at low applied fields. A more aggressive acceleration model is required to make accurate lifetime predictions at low fields.

**PS.BD5**  
**Effect of Line-Overlay and Via-Misalignment on Dielectric Reliability for Different Patterning Schemes, K. Croes, I. Ciofi, D. Kocaay, Z. Tokei and J. Bommels, imec**

Advanced patterning schemes were compared with respect to misalignment on dielectric reliability. The patterning schemes compared in this study are litho-etch-litho-etch and self-aligned-double-patterning. For typical intrinsic reliability parameters, in comparison with the ideal case of 0nm misalignment, the self-aligned-double-patterning scheme with a 3σ misalignment of 6nm leads to a Vmax reduction of 26%. The additional overlay errors induced by the litho-etch-litho-etch patterning scheme leads to a reduction of Vmax by 43%.

**PS.CA2**  
**DC / AC BTI Variability of SRAM Circuits Simulated Using a Physics-Based Compact Model, T. Naphade, P. Verma, N. Goel and S. Mahapatra, Indian Institute of Technology Bombay**

A physics-based compact model is developed to predict BTI induced VT distribution under DC and AC stress in HKMG devices. The model is verified against measured data. Device level delta VT and VT distributions are generated for DC stress, and for different duty cycles for AC stress. Impact on 6T and 8T SRAM cells is investigated for read/write operations after different activity conditions and long time failure probabilities are obtained.

**PS.CA3**  
**On-Chip Aging Compensation for Output Driver, V. Kumar, STMicroelectronics Pvt. Ltd.**

As the CMOS technology is shrinking the impact of aging degradation on I/O buffer especially on output driver is getting accelerated due to signal integrity and transmission line effects because it is directly interfacing with peripheral devices. In this paper an on-chip aging compensation technique for CMOS output driver is proposed which reduces the impact of aging on output driver by 70% after 10 years of operation.

**PS.CA4**  

A NBTI compact model considering the interface-state generation and hole-trapping mechanisms has been proposed in spite of different materials and processes. 8 model parameters describes universal
characteristics of the MOSFET degradation simply as a function of the gate oxide field ($E_{ox}$). By implementing the NBTI model into the compact model HiSIM, the circuit delay degradation is predicted, where the interface state generation and hole-trapping mechanisms dominate the degradation at low and high frequency operation respectively.

PS.CA5

In this paper, BTI reliability at the circuit-level is compared with the scaling point of view from planar FET to advanced 3-D FinFET nodes in combination with the time-zero variability aspect. Circuit-level insights are given based on case study simulations of Ring Oscillators (ROs) at commercial-grade 28nm planar and research-grade 14, 10, 7nm FinFET technology nodes for several FET channel materials (e.g. SiGe, Ge, III-V, etc.).

PS.CA6
A Reliability Lab-on-chip Using Programmable Arrays, P. Pfeifer, B. Kaczer* and Z. Pliva, Technical University of Liberec, *imec

This paper presents a new concept of a reliability lab-on-chip. It is shown how multiple test structures, including the measurement blocks, can be ad-hoc created and evaluated directly on a Field-Programmable Gate Array (FPGA) chip. Results from measurements including 28 nm processes are presented as well.

PS.CA7
A Physical and Scalable Aging Model For Digital Library Characterization, H. Kufluoglu, C. Cirba, M. Chu, M. Chen, S. Datla and V. Reddy, Texas Instruments

Multi-Voltage-Temperature End-of-Life (MVT-EOL) models enable accurate assessment of circuit-level BTI and CHC degradation during digital library characterization. A physics-based MVT-EOL aging model has the advantage of its data, modeling, and computational requirements not being as demanding compared to sophisticated aging simulators. The MVT-EOL is compatible with fast SPICE simulators and can thus efficiently handle large circuits. Aging under dynamic VDD scaling is incorporated through an equivalent voltage ($V_{EFF}$) condition and compares well with circuit data.

PS.CA8
System-Level Modeling of Microprocessor Reliability Degradation Due to BTI and HCI, C.-C. Chen, S. Cha, T. Liu, and L. Milor, Georgia Institute of Technology

Negative bias temperature instability (NBTI), positive bias temperature instability (PBTI) and hot carrier injection (HCI) are leading reliability concerns for modern microprocessors. In this paper, a framework is proposed to analyze the impact of NBTI, PBTI and HCI on state-of-art microprocessors, and to accurately estimate microprocessor lifetimes due to each wearout mechanism.

PS.CA10
The Impact of High Vth Drifts Tail And Real Workloads on SRAM Reliability, D. Angot, V. Huard, M. Quoirin, X. Federspiel, S. Haendler, M. Saliva and A. Bravaix*, STMicroelectronics, *IM2NP-ISEN

SRAMs are often very challenging both on process side (due to small dimensions) and on design side (due to performance request). As a consequence, managing their reliability is of prime importance. This
paper presents a large dataset of both measurements at device and bitcell levels and monte-carlo simulations. A fully analytical model is proposed to predict accurately Vmin distributions for different cut sizes. The impact of BTI variability modeling and workloads on predictions is analyzed.

**PS.CD1**


The Photo Emmission Microscopy (PEM) technique was used to characterize the spatial distribution of electroluminescence (EL) to locate the possible failure site in degraded AlGaIN/GaN HEMTs. The site-specific structural and chemical analysis technique were performed to analysis the relationship between the distribution of the EL and the structural damage of device. A new failure mechanism, related to thermal mismatch, of the AlGaIN/GaN HEMTs was firstly identified and reported.

**PS.CD2**


Dynamic capacitance dispersion techniques are implemented to characterize the interface states of Al2O3/AlGaIN/GaN. Two types of device structures, are used in the experiments. Interface trap states parameters in both devices have been confirmed. Experimental results demonstrate that gate recess process can induce extra traps with shallow levels at Al2O3/AlGaIN interface due to the damage on the surface of AlGaIN barrier layer resulted from reactive ion etching (RIE).

**PS.CD3**

**Enhancement of Off-State Breakdown Voltage in AlGaIN/GaN HEMTs Using a High-k Thick Passivation Layer**, H. Hanawa, A. Nakajima and K. Horio, Shibaura Institute of Technology

We perform a two-dimensional analysis of breakdown characteristics in AlGaIN/GaN HEMTs as parameters of relative permittivity of the passivation layer er and its thickness d. It is shown that the off-state breakdown voltage increases as er and d increase, because the electric field at the drain edge of the gate is reduced. It is concluded that AlGaIN/GaN HEMTs with a high-k and thick passivation layer should have high breakdown voltages.

**PS.CD4**


This paper reports on trap-related shifts of the transfer curve and threshold voltage of GaN HEMTs under switched bias operating life, and reverse and forward DC bias stress. Opposite polarity threshold voltage shifts under operating life versus reverse bias conditions is explained by drain current transients. A model describing trapping behavior and the role of field plate design and its use to suppress the extent of shifts of the transfer curve.
PS.CD5

TDDDB Breakdown of th-SiO$_2$ on 4H-SiC: 3D SEM Failure Analysis, M. Hayashi, K. Tanaka, H. Hata, H. Sorada, Y. Kanzawa and K. Sawada, Panasonic Co., Ltd

We investigated SiO$_2$ void volumes using continuous observation by FIB-SEM and constructing their 3D images. We provided a new insight into the impact of SiO$_2$ void volume on the 4H-SiC TDDDB failure. The small SiO$_2$ void plays a very important role in the degradation of TDDDB reliability. The present 3D SEM technique is very useful in the visualization of SiO$_2$ voids as well as in the investigation of TDDDB failure mechanism.

PS.CD6

Electrical Characterization and Reliability Analysis of Al$_2$O$_3$/AlGaN/GaN MISH Structure, J. Wu, X. Lu, S. Ye, J. Park, and D. Streit, University of California, Los Angeles

We present here a comprehensive electrical characterization and reliability analysis of Al$_2$O$_3$/AlGaN/GaN metal insulator semiconductor heterostructure (MISH). MISH capacitors are characterized using C-V, I-V, constant-current stress and TDDDB measurements. It is shown that 1) interface states with mid-level density exist near conduction band; 2) F-N tunneling dominates in oxide current transport; 3) gate voltage rises due to reduced oxide field during constant-current stress; 4) a Weibull slope of 5.78 of Al$_2$O$_3$ dielectric can be extracted.

PS.CD7


Degradation mechanisms of AlGaN/GaN high electron mobility transistors under step-tress were investigated in this paper. Although gate current degraded suddenly beyond a certain stress voltage in the devices with large gate-to-source distance, no obvious “critical voltage” could be found when the gate-to-source spacing is small. It is supposed that surface leakage current becomes crucial when the gate and source electrodes come near, and the degradation of gate current induced by inverse piezoelectric effect is shield.

PS.CD8

Observation of Threshold Voltage Instabilities in AlGaN/GaN MIS HEMTs, K. Zhang, X. Ma and Y. Hao, Xidian University

We report the investigation of threshold voltage (Vth) instability of AlGaN/GaN metal–insulator–semiconductor (MIS) HEMTs with SiN gate dielectric under forward gate bias stress. A systematic step stress-recovery experiment is implemented to study the charging and discharging kinetics of pre-existing defects. A two-step trapping process is observed: electron fast trapping into dielectric or SiN/AlGaN interface by tunneling through the thin AlGaN layer and slow dynamics with a logarithmic time-dependence of the Vth shift.

PS.CD9

Characterizing Stress And Temperature And Its Impact On The Degradation of AlGaN/GaN HEMTs, S. Choi, J. Jones, M. Rosenberg*, E. Heller**, D. Dorsey**, R. Vetury**, W. King and S. Graham, Georgia Institute of Technology, *University of Illinois, **Air Force Research Laboratory, ***RFMD

In this work, both Raman Spectroscopy and Scanning Joule Expansion Microscopy are used to measure the temperature and strain in AlGaN/GaN HFET devices. Electro-thermo-mechanical model is then used
to correlate with the experimental measurements and used to predict the stress distribution in the devices. A combination of off state and on state testing shows that the onset of failure is related to the total stress state arising from residual, inverse piezo, and thermal stresses.

**PS.CD10**
Comparing the Active and Passive Cooling of AlGaN/GaN HEMTs: Microchannel Cooling Versus High Conductivity Substrates, X. Chen, F. Donmezer, S. Kumar, E. Heller*, D. Dorsey* and S. Graham, Georgia Institute of Technology, *Air Force Research Laboratory

Methods to reduce the hotspot temperature in AlGaN/GaN HMETs are critical to the improvement in thermal management and reliability of these devices. In this work, we evaluate the thermal performance of AlGaN/Gan HEMTs on Si, SiC, and diamond substrates and compare them to substrates with integrated micro channel cooling. The data show that integrated micro channels with pin fin architectures in SiC substrates can outperform devices made on 100 um thick diamond substrates.

**PS.CD11**
High-Voltage Double-Pulsed Measurement System for GaN-Based Power HEMTs, D. Bisi, A. Stocco, M. Meneghini, F. Rampazzo, A. Cester, G. Meneghesso and E. Zanoni, University of Padova

A fully customable high-voltage pulsed system capable of double-pulsed I-V and time-resolved drain-current transient characterization is presented. The system allows a comprehensive characterization of the charge-trapping affecting the dynamic performances of GaN-based power HEMTs under high-voltage operational biases. We discuss the main issues of a high-voltage pulsed- and transient-characterization, propose solutions for reliable measurements and data acquisition, and demonstrate the effectiveness of the system through the description of a case-study.

**PS.CP2**

Moisture concentration at the critical interface is the key parameter as far as moisture sensitivity of a plastic package is concerned. Using a simple moisture diffusing model, this parameter allowed us to predict the optimal baking time at 125°C for e.g. P-DSO14: 4-16 hours, depending on the considered interface. The theoretical predictions agree well with the experimental results. On the other hand, the standard IPC/JEDED J-STD-033C recommends the distinctly longer baking time of 43 hours.

**PS.EL1**
Improving ESD Robustness of Stacked Diodes with Embedded SCR for RF Applications in 65-nm CMOS, C.-Y. Lin, M.-L. Fan*, M.-D. Ker*, L.-W. Chu**, J.-C. Tseng** and M.-H. Song**, National Taiwan Normal University, *National Chiao Tung University, **Taiwan Semiconductor Manufacturing Company

To protect the radio-frequency (RF) integrated circuits from ESD damage in nanoscale CMOS process, the ESD protection circuit must be carefully designed. In this work, stacked diodes with embedded silicon-controlled rectifier (SCR) to improve ESD robustness was proposed for RF applications. Experimental results in 65-nm CMOS process show that the proposed design can achieve low parasitic capacitance, low turn-on resistance, and high ESD robustness.

**PS.EL2**
Evaluation of Geometry Layout and Metal Pattern to Optimize ESD Performance of Silicon Controlled Rectifier (SCR), Z. Wang and J. Liou, University of Central Florida
We investigate the geometry layout and metal pattern in order to seek robust and optimized electrostatic discharge (ESD) performance for the silicon controlled rectifier (SCR). Parallel and crossing topologies, and different emitter lengths of the parasitic bipolar transistors, finger widths, and finger numbers are shown to significantly affect not only the ESD robustness but also the holding voltage of SCR. This paper provides useful guidelines to ameliorate the SCR performance for ESD protection applications.

PS.EL3

The proposed MLT-NLDMOS have been successfully verified in 0.35μm CDMOS/FDMOS process, which can lower trigger voltage about 11%. The layout structure is simple and clear by separating the source and bulk side into three parts, and there is no need to add extra mask layer, additional process step or any accessory circuit. In addition, the HBM and the MM ESD levels are 4.5KV and 325V, respectively.

PS.EL4

A DC and pulse stress electro-thermal model that can well describe the dynamic thermal behaviors of most interconnections fabricated in CMOS technology is derived and demonstrated. This model provides for the first time a simple methodology to evaluate the time dependent temperature and resistance of the interconnection under an applied voltage stress, especially critical to E-Fuse development.

PS.EL5
Study on ESD Protection Design with Stacked Low-Voltage Devices for High-Voltage Applications, C.-T. Dai and M.-D. Ker, National Chiao-Tung University

ESD protection with stacked low-voltage (LV) devices are proposed to form an area-efficient design for high-voltage (HV) applications in a 0.25-µm HV BCD process. With stacked configuration, LV devices can provide scalable triggering voltage (V\text{t1}) and holding voltage (V\text{h}) for various HV applications. Experimental results in silicon have verified that the stacked LV devices can exhibit a higher ESD robustness per unit layout area as comparing to the ESD clamp circuit with HV device.

PS.ER1
New Methodology for Drift Analysis on Reliability Trial, M. De Tomasi, R. Enrici Vaion, L. Cola, P. Zabberoni and A. Mervic, STMicroelectronics

Reliability requirements are becoming more and more demanding and drift analysis after reliability stress is increasing its importance as key process to judge reliability results, in accordance to robust validation guidelines. This work is focused on the developing of a new methodology to perform drift analysis after reliability stress in order to assess if a meaningful drift is present between data before and after stress.

PS.ER2
A model is derived to calculate component effective lifetime and failure rate (FIT) for arbitrary use conditions (temperature and voltage). The overall component failure rate vs time for a 28nm technology is demonstrated to be Weibull with slope ~0.34 indicating early failures still dominate instead of wear-out. The effective $E_a \approx 0.69\text{eV}$ and the effective voltage acceleration parameter $V_{AP} \approx 20$ but can range from 17 power-law to 23.5 exponential dominated by NBTI or PBTI assisted extrinsic failures.

**PS.ER4**  
*Is Your Silicon Reliable? A System Approach of Silicon Qualification Methodology*, H. Yu, A. Curtis, A. Marathe and R. Master, Microsoft Corporation

An interactive custom silicon qualification methodology is presented to address the reliability and quality challenges faced by system companies and their custom silicon component suppliers. The methodology helps to increase transparency, mutual understanding, identify gaps and set appropriate expectations between them. Two XBOX360 case studies are described to demonstrate the benefits of the interactive qualification methodology with silicon suppliers compared to an independent and decoupled qualification effort from silicon suppliers without consideration of system requirements. A Kinect CMOS image sensor case study shows the effectiveness of the proposed interactive system approach of silicon qualification methodology, and its implementation that leads to a win-win situation for both the system and component companies. A new CMOS image sensor qualification methodology is introduced.

**PS.FA1**  

Current and temperature aging have been conducted on flip-chip LEDs with Al-Ni-Ti-Au n-contacts. Electrical and optical characteristics have been followed during aging and a forward voltage increase has been observed. Cross sections have been made on representative aged samples. For LEDs with a forward voltage shift, in the n-contact area, Au-Al interdiffusion leading to a possible formation of Au-Al intermetallic compounds has been observed. We propose to analyze this mechanism and its consequences on reliability.

**PS.FA2**  

We report a method for evaluating graphene interconnect wiring structure by conductive atomic force microscopy (C-AFM), which enables direct observation and measurement of the 2D-resistance distribution of multi-layer graphene (MLG) on Ni. The coverage of MLG on Ni was evaluated by comparing C-AFM image with SEM observations. Also, we confirmed conduction paths of MLG/Ni interconnect. Process dependence of MLG shows that lower local resistance corresponds to higher G/D ratio in Raman spectra.

**PS.FA3**  

We tried to observe transmitted photon from top surface in avalanche breakdown of power MOSFET using Time Resolved Emission (TRE) microscopy microscopy. The sensitivity of TRE microscopy is
higher than that of PEM, so it has potential for detecting only a few photons which are transmitted through the electrode metal. A sudden increase of photon counts was observed at the same time as start of avalanche breakdown in MOSFET.

PS.FA4

In this work we present an adaptive grinding and polishing technique that incorporates in-situ measurement of thickness and flatness into a five axis CNC machine. The CNC performs discrete measurements of the backside surface of the packaged die and the thickness uniformity of the silicon using a non-contact optical technique. Analysis software fits and filters the measurement data to construct a continuous, three dimensional (3D) model of the circuit layer.

PS.GD1
Demonstrating Individual Leakage Path from Random Telegraph Signal of Stress Induced Leakage Current, A. Teramoto, T. Inatsuka, T. Obara, N. Akagawa, R. Kuroda, S. Sugawa and T. Ohmi, Tohoku University

We evaluated stress induced leakage current of 87344 1μm2-MOSFETs with the extremely small current range of 1e-17 to 1e-13 A. We extracted the leakage current from the random telegraph signal of gate current. Each current value indicates the absolute current of one individual localized leakage path, and these large leakage currents become bit error in flash memories. The evaluation method and the results are useful for high reliable process and design technologies in MOS devices.

PS.GD2

A new wafer-level reliability qualification methodology is proposed. Unlike conventional method, the new technique only requires a single device and the total test time can be controlled within 2 hours. The new method can be an effective tool for fast reliability screening during process development.

PS.GD3

Trap generation (TG) is directly estimated during N and P BTI in MOSFETs with different HKMG stacks. NBTI-TG is due to Si/IL interface degradation. PBTI TG occurs at IL/HK interface and HK bulk, former having more impact on VT degradation. It’s observed that TG at Si/IL interface for NBTI and at IL/HK transition layer for PBTI are governed by similar dynamics. Relative impact of TG and TP on VT degradation is shown for different EOT scaled devices.

PS.GD4
We report on a methodology to assist fabrication process development using high and low thermal budget fabrication flows for high-k n-MOSFETs. This methodology is supported by simulations allowing extracting defect characteristics by fitting measurement data, specifically SILC, PBTI, and MFCP. The contributions of pre-existing and stress-induced defects in gate stacks on device performance are examined. Information on defect distributions in the as-fabricated and post-stress devices directs process optimization efforts to the problematic gate stack regions.

**PS.GD5**

**Voltage Pulse Stress Effect on Gate Stack TDDB Distributions at Nanometric Scale: Consequence on Aging by ESD**, R. Foissac, S. Blonkowski, M. Gros-Jean, and M. Kogelschatz*, STMicroelectronics, *University of Grenoble

In this work an AFM in conductive mode is used under ultra-high vaccum to study the effect of the pre stress pulse height and duration on the TDDB and VBD statistic distributions of a 1.4nm thick SiON gate oxide layer. An extrapolation formula for the mean TTF evolution, i.e. ESD ageing, as a function of pre stress pulse characteristics is deduced.

**PS.GD6**


This paper deals with AC/DC effect on nMOS TDDB & PBTI using suitable OTF monitoring methodologies. First, TDDB dependences on frequency and duty cycle are studied. For frequencies above 100Hz, TBD is shown to depend significantly on these two parameters. On the other hand, to evidence a possible effect of trapping on TDDB, PBTI dependences on frequency and duty cycle are also studied using fast BTI measurement. Finally, trapping/detrappping mechanisms fail to explain TDDB observations.

**PS.IT1**


Negative shift of resistance during stress migration was observed in Cu-based, dual-damascene technologies. One significant reason is caused by via copper crushing through the barrier layer into copper trench underneath, which means that via location acts main role in large shrinking of via resistance. Besides, negative shift of via resistance is found to be increasing with baking time, which indicates that anneal effect can also play an important role in decreasing via resistance.

**PS.IT2**

**Electromigration Analysis of Full-Chip Integrated Circuits with Hydrostatic Stress**, P. Gibson, M. Hogan and V. Sukharev, Mentor Graphics

Interconnect reliability requirements of advanced process nodes have eroded design margins, increasing susceptibility to electromigration. Elaborate design requirements are needed to compensate for the lack of suitable materials to protect against such effects. Traditional Electronic Design Automation (EDA) verification tools exhibit significant difficulty when trying to validate these rules. We introduce a design context-aware interconnect reliability solution for full-chip electromigration analysis which considers current density, Blech Effect and nodal hydrostatic stress analysis for failure prediction.
**PS.IT3**


SM failure mode in the metal line was explored. In this work, we further investigate SM behavior in different process at Cu/low-k and Cu/ESL interfaces. We observed vacancies from the wide metal plate initially migrate through Cu grain to Cu/low-k interface, then move to Cu/ESL interface, and eventually form voiding in the narrow metal line. SM failure mode can be eliminated through a new nose structure with special narrow metal line design consists of two branch widths.

**PS.IT4**


A new design concept is to modify the shape of these lines. The use of slots especially of octahedron slots demonstrates a better robustness towards electromigration in upper metallization layers. Another benefit is the good reliability under pulsed DC conditions. In addition with slotted metal in all metallization layers stress due to thermal expansion can be reduced by keeping the lifetime at an adequate level.

**PS.IT5**

Model Based Method for Electro-Migration Stress Determination in Interconnects, E. Demircan and M. Shroff, Freescale Semiconductor Inc.

Electro-migration (EM) failure in interconnects is one of the most important reliability considerations in current advanced semiconductor technologies. In this paper we present a novel methodology based on a model-based approach where EM risk can be assessed for any interconnect geometry through an exact solution of the fundamental stress equations. This approach eliminates the need for complex look-up tables for different geometries and can be implemented in CAD tools very easily.

**PS.IT6**


Although the introduction of Mn alloyed with Cu has shown some promise to improve the reliability, it is still non-trivial to have a complete solution in terms of engineering as scaling continues. In order to compensate for the intrinsic weakness of the Cu/barrier layer interface surface and engineering uncertainties, it is necessary to consider different pathways to meet the reliability standards. In this paper we study the impact of via arrangement on the electromigration related performance and investigate failure statistics as a function of the failure criteria.

**PS.MY1**

Stacked Etch-Induced Charge Loss in Hybrid Floating Gate Cells using High-k Inter-Gate Dielectric, M.B Zahid, L. Breuil, R. Degraeve, P. Blomme, C.-L. Tan, J. Lisoni, G. Van den bosch and J. Van Houdt, IMEC

In contrast to capacitors, scaled cells are subject to stacked etch of CG and FG, possibly leading to etch damage at the cell sidewall. In this paper, we investigate the stacked etch-induced charge loss in multi-layer IGD cells with HFG and how this is influenced by the CG material (5nm ALD-TiN, Poly-Si and Amorphous Si :"a-Si").
PS.MY2

Statistical characterization of two-level random telegraph noise (RTN) amplitude distribution in a hafnium oxide resistive memory has been performed. We find that two-level RTN in HRS exhibits a large amplitude distribution tail, as compared to LRS. A correlation between an RTN trap position and RTN amplitude is found. Our characterization and simulation show that RTN traps in a rupture region of a hafnium oxide film are responsible for an RTN large-amplitude tail in HRS mostly.

PS.MY3

Write disturb on half-selected (HS) cells are investigated through electrical measurement and large-scale array simulation. The experimental results collected from the individual devices under constant stress voltage and consecutive pulse operation are correlated with HS cells in large-scale arrays based on a physics-based compact model. The impact of write/read disturb on HS cells at different locations of the arrays are analyzed. Design guidelines based on the experimental data and HSPICE simulations are presented.

PS.MY4

This work presents a physics-based model for RTN in RRAM, based on trap-induced depletion of the conductive filament (CF). The model accounts for size-dependent RTN, which is explained by partial and full depletion of the CF. Voltage-dependent RTN is described by localized Joule heating, as supported by RTN experiments at variable temperature.

PS.MY5

Hafnia-based RRAM, demonstrating high-density low-power operations and fast switching, are promising for non-volatile memory application. Nonetheless certain stochastic characteristics, specifically cycling variability and RTN, are hindering device scaling, delaying full industrial introduction of RRAM. Here, we investigate RTN and cycling variability in HfOx RRAM from both experimental and theoretical standpoints. We analyze statistical data measured on different RRAM stacks at various operating conditions using physical simulations, demonstrating the uncorrelated nature of RTN and cycling variability.

PS.MY6
Modification condition for hydrogen effect has been researched, which affects data retention characteristics of NAND flash in scaling-down. Hydrogen, which increases traps, prevents perturbation before cell contact formation. After cell contact formation, out-gassing engineering is applied so that maximized data retention characteristics we can acquire. It can be modeled as an effect with or without hydrogen removal path. Hydrogen engineering result confirmed up to sub 3x–1xnm NAND suggests a good direction in vertical NAND structure.

PS.MY7
Bit Error Rate Analysis in Charge Trapping Memories for SSD Applications, A. Grossi, C. Zambelli and P. Olivo, Università di Ferrara

Charge Trapping (CT) memories are one of the most promising candidates in replacing Floating Gate (FG) NAND Flash memories because of a better scalability and high interest for 3D NAND approaches. In this work Recovery and Refill algorithms are shown to reduce BER with respect to the ISPP algorithm in CT-NAND. By combining this with a Read Retry error reduction procedure it is possible to get BER values that make CT-NAND feasible for SSD applications.

PS.MY8

We present for the first time an in-depth reliability investigation of T-RAM cells considering read failure, data retention and endurance, providing a clear picture of the physical processes involved. Results reveal a successful operation exploiting the trade-off between the retention requirements for state-0 and state-1 and highlighting a negligible impact of electrical stress up to very high cycling doses.

PS.MY9

Endurance is one of the key reliability metrics for RRAM. In this work, we develop a phenomenological model for estimating the probability distribution of endurance failure in reset stage (low to high resistance state (LRS → HRS)), taking into account factors such as the pulse voltage, pulse duration, compliance level, activation energy, temperature, filament shape etc... The 2D percolation model for dielectric breakdown is used as the backbone for endurance model formulation.

PS.MY10

We demonstrate reliable RRAM operation by controlling the forming energy via short voltage pulses (picosecond range) which eliminates the need for a current compliance element. We further show that the dissipated energy during forming and SET/RESET processes plays a critical role. Multiple-pulse forming is also investigated as a method to further tighten the control of forming energy with promising endurance results.

PS.PI1

We propose a circuit model for investigating the charging damage in FDSOI devices as a function of the physical parameters of the plasma and the antenna characteristics. The model succeeds in predicting the damage obtained by experimental measurements.

**PS.PI2**

Theoretical investigations are presented to study the formation of defects in III-V fins grown using the aspect ratio trapping technique for the first time. We show that during the growth of the III-V, the formation of intermediate chemical states with the precursors leads to the creation of in-diffused Mg/Zn and Al2O3 sub-oxide. Our prediction is consistent with the experimental observations. These defects could be causes to degrade the electrical reliability of III-V FinFETs.

**PS.PI3**
**Effect of I/O Oxide Process Optimization on the NBTI Dependence of \( T_{in} \), Scaling for a 20 nm Bulk Planar Replacement Gate Process, C. Tian, G. La Rosa, W. Liu, M.-J. Jin**, W. Lai, S. Siddiqui, F. Guarin, H. Kothari***, W. McMahon\(^\wedge\), S. Uppal\(^\wedge\), B. Linder*, and V. Narayanan*, IBM Microelectronics, *IBM TJ Watson Research Center, **Samsung Electronics, ***STMicroelectronics, \(^\wedge\)GLOBALFOUNDRIES**

We present results on the beneficial effect of an additional thermal treatment on the NBTI of an I/O thick oxide process in 20nm Replacement Gate High-\( \kappa \) Metal Gate technology. We will show the NBTI induced \( V_t \) shift yields a weak \( T_{in} \) dependence for the as-grown thermal oxide, which is inconsistent with well known NBTI dependence on \( E_{ox} \), but an additional high temperature anneal recovers the \( E_{ox} \) dependence. The results and cause will be discussed.

**PS.PR1**
**System-Level Estimation of Threshold Voltage Degradation due to NBTI with I/O Measurements, S. Cha, C.-C. Chen and L. Milor, Georgia Institute of Technology**

With the scaling of CMOS technology, Negative Bias Temperature Instability (NBTI) and Process Variations (PV) are serious issues for transistors. We present a method to determine the initial average channel length and threshold voltage for individual chips, together with NBTI model parameters through I/O measurements. We determine models which are used to extract PV and NBTI parameters. We calculate the lifetimes for each chip individually using calibrated NBTI models, accounting for process variations.

**PS.PR2**
**Using Thermal Cycle And Temperature / Voltage Testing To Reduce The Incidence of Resistive / Open Reliability Defects, A. Swift, IBM Microelectronics**

The continued scaling of CMOS technologies has challenged the capability of “traditional” reliability defect screens. The increases in power due to scaling has diminished the effectiveness and increased the cost of performing accelerated voltage based screens such as Burn-in. Through experimentation, it was determined that the use of Thermal Cycle and temperature/voltage corner testing significantly diminished
the magnitude of opens/resistive mechanisms and also afforded some screening of “traditional” “shorting” mechanisms.

PS.PR3

Similar to ASH, the study of Vmin-shift induced failure on AP is stretched to “set level” stress test. This test enables to filter out unscreened functional or power related early fails particularly with high frequency and heavy duty scenario-based software test and as a result, field failure rate is significantly reduced. We’ll discuss the system level stress tests and its perspective as the current and future qualification required for new product introduction of high-speed mobile applications.

PS.PR4

As technology continues to shrink, minimizing SRAM operating voltage (Vmin) have faced a critical challenge due to increasing threshold voltage variation. Therefore assist circuits have become a foreseeable solution for Vmin improvement. In this work, we characterized Vmin behaviors with read-write assist circuit before and after high temperature operating life stress. Our study demonstrated that assist circuits not only improved Vmin at time zero, but also beneficial to suppress BTI induced Vmin degradation after HTOL.

PS.PR5
Setting Use Conditions for Reliability Modeling, R. Kwasnick, P. Polasam and A. Lucero, Intel Corporation

Use conditions (UCs) are necessary inputs for knowledge-based qualification reliability modeling calculations, and are implied by standard-based qualification stress conditions. We describe a method for setting CPU UCs. A sampled distribution of field data is analyzed, accounting for the reliability model Weibull shape factor. This is integrated with other information to determine a reference value for modeling with appropriate conservatism. We present application to notebook PCs for both silicon and thermo-mechanical CPU wearout mechanisms.

PS.SE1
65 nm Fault Tolerant Latch Architecture Based on Transient Propagation Blocking, M. Glorieux, S. Clerc, G. Gasiot, J.-L. Autran* and P. Roche, STMicroelectronics, *Aix-Marseille University and CNRS

A new solution is proposed to protect sequential logic against single event effects. This hardening mechanism blocks the propagation of voltage transient generated by ionizing particles and limits delay penalties as only one transistor is added in the data path. A flip-flop has been designed with this new latch in 65 nm technology and accelerated protons tests show $4 \times$ soft-error-rate reduction.

PS.SE2
Impact of Body Bias on Soft Error Tolerance of Bulk and Silicon on Thin Box Structure in 65-nm Process, K. Zhang, Y. Manzawa and K. Kobayashi, Kyoto Institute of Technology
We analyze the soft error tolerance of DFF in 65-nm bulk and SOTB (Silicon on Thin BOX) process. The experimental results reveal that the soft error rate in the bulk structure is increased, while the one in SOTB structure is decreased by increasing the reverse bias. The results from device-simulation show that the collected charge of bulk structure is increased, while the collected charge is decreased in SOTB by increasing the reverse bias.

PS.SE3

We propose a method that prevents single event latchup (SEL) using deep P-well on P-substrate. To confirm the effectiveness of the proposed method, SEL and single event upset (SEU) are evaluated for three well configurations; double-well, ordinary triple-well and the proposed deep P-well on P-substrate. Neutron irradiation test shows that the proposed method achieves SEL prevention without SEU increase.

PS.SE4

Alpha-particle and heavy-ion soft-error cross section response of multiple D-Flip-Flop (DFF) designs fabricated in a 32 nm CMOS SOI technology are compared. Specifically, the transistor stacking hardening technique, with a focus on minimizing area penalty, is compared to unhardened DFF and dual interlocked storage cell (DICE) designs. The stacking hardened DFFs show over two orders of magnitude increase in hardness to soft errors and less than 50% area penalty compared to unhardened D-flip-flop designs.

PS.SE5

Alpha, high-energy proton, neutron, and heavy-ion experimental results of 30 different flip-flops in a 28-nm bulk CMOS process are compared. The results show the spectrum of soft error rates a designer may see for hardened and non-hardened flip-flops at the 28-nm bulk CMOS technology node.

PS.SE6
**SER/SEL Performances of SRAMs in UTBB FDSOI28 and Comparisons with PDSOI and BULK Counterparts**, G. Gasiot, D. Soussan, M. Glorieux, C. Bottoni, and P. Roche, STMicroelectronics

This work presents alpha and neutron SER characterization of a 28nm commercial Fully Depleted SOI technology predisposed to consumer applications. Its intrinsic SER hardness is as well compared to known high-reliability Partially-Depleted SOI technologies.

PS.XT1
**Similarity and Difference in Temperature Dependent Recovery of HCS and NBTI**, Y. Yonamomo, Hitachi, Ltd.
We investigated the temperature dependence of recovery behavior of pMOSFETs after hot carrier stress (HCS) and negative bias temperature stress (NBTS) from the recovery activation energy distributions of threshold voltage shifts ($E_r^{V}$) and of interface states ($E_r^{D}$). Both $E_r^{V}$ and $E_r^{D}$ were composed of two elements, recoverable- and permanent components ($R$ and $P$). $R$ and $P$ can explain the temperature dependent recovery after HCS and NBTS. The degradation mechanism is also discussed.

**PS.XT2**

**BTI Recovery in 22nm Tri-Gate Technology**, S. Ramey, J. Hicks, L. Suriyasena* and S. Novak, Intel Corporation

BTI recovery in tri-gate devices matches data and model predictions from planar devices, indicating a consistent physical basis for the mechanism and no influence from transistor architecture features such as crystal orientation and fin corners. This consistency enables extending existing planar models to capture temperature and voltage dependencies. A new experimental technique allows extraction of an effective activation energy for recovery. The observation of complete recovery demonstrates that no permanent damage occurs during stress.

**PS.XT3**


Frequency dependency of the NBTI in wide frequency range (10 KHz ~ 500 MHz) is investigated using on-chip test structure. Statistical meaningful AC/DC lifetime ratios are extracted after stress and show a non-monotonic behavior. RTN trap analysis reveals that trap located near interface with time constant 1e-10~1e-4s are responsible for such behavior. A model from trap occupancy of defects point of view is also proposed to justify non-monotonic AC/DC ratio in wide frequency range.

**PS.XT4**


In this paper, we performed that the gate bias-temperature-stress (VG-BTS) induced off-state leakage. The physical model is attributed to the positively trapped charge and interface trap in STI SiN-liner and interface. Although long-term high operational gate voltage with STI SiN-liner cannot be avoided as in fast program/erase requirement of flash memory, we provided the lifetime predicted method of $I_{off}$ and design suggestions for the reliable flash memory developed solutions in the future.

**PS.XT5**

**The Effects of Biaxially-Tensile Strain to Properties of Si/SiO$_2$ Interface States Generated by Electrical Stress**, W. Cai, M. Takenaka and S. Takagi, The University of Tokyo

The effect of biaxially-tensile strain to the properties of Si/SiO$_2$ interface states generated by FN stress have been systematically investigated. In order to accurately evaluate $D_i$ in MOS capacitors and FETs including strained-Si (sSi)/SiGe hetero-interfaces, the conductance method and the S-factor method have been properly modified. It is found that strain does not change the properties of SiO$_2$/Si interface states.

**PS.XT6**

In this work, we report for the first time a process dependence of positive bias temperature instability (PBTI) under AC and DC stresses in a recent HKMG technology.

**PS.XT7**
**Combined Ramp Voltage Stress and Constant Voltage Stress for Optimal BTI Voltage Acceleration and Lifetime Modeling,** B. Linder and T. Ando, IBM

BTI is often screened using a fast Ramp Voltage Stress (RVS) while Constant Voltage Stress (CVS) is typically utilized for lifetime projection. Because the voltage is ramped during an RVS stress, an RVS trace yields an extremely detailed understanding of the voltage dependence of BTI. This paper highlights the pitfalls of relying on just CVS for BTI lifetime projections and also demonstrates the complimentary nature of RVS and CVS for lifetime modeling.

**PS.XT8**

Self-heating (SHE) is becoming a key factor in roadmap planning. SHE will become worse due to increased electric field density and reduced silicon volume available for heat removal. Most simulations of this effect lack experimental proof. In this study, i) we propose a unique measurement technique for self-heating and use it to assess self-heating in planar devices, ii) compare and verify these results with 3D finite-element simulations and iii) provide perspectives for upcoming FinFET nodes.

**PS.XT10**

Studies on DPBTI stressing shows greater transformation of shallow electron-trap states to deeper levels at a higher frequency. To consistently explain the result, it is necessary for the transformation to occur via an intermediate state. At a sufficiently high frequency (short relaxation phase), the electron trap concerned may remain in the intermediate state throughout DPBTI stressing, and thus the likelihood of transition to the final deep state is increased.

**PS.XT11**
**Comprehensive Experimental Study of NBTI under Compressive and Tensile Strain,** W. Wu, C. Liu, J. Sun, Y. Shi and Y. Zhao*, Nanjing University, *Zhejiang University

We have comprehensively studied the effects of all four types of strains (uniaxial tensile strain, uniaxial compressive strain, biaxial tensile strain and biaxial compressive strain) on the NBTI reliability behaviors of Si pMOSFETs. For the first time, it has been experimentally confirmed that both uniaxial and biaxial compressive strains could improve the NBTI reliability of Si pMOSFETs. The NBTI reliability was degraded in both uniaxial and biaxial tensile strained Si pMOSFETs.

**PS.XT12**
One of the main causes of parameter degradations in recent technologies is (HCI), a progressive wear out phenomenon whose understanding and modeling has become mandatory in current CMOS nodes. Therefore, we present in this paper an experimental analysis of HCI degradation for FDSOI MOSFETs. The carrier energy and bulk bias dependencies are modeled according to our recent findings through a simple HC model based on existing physical theories applied to the specificity of FDSOI technology.

PS.XT13

We propose a new method to determine the lateral position of border traps in MOSFETs. The approach exploits the fact that the drain bias dependence of the trap-induced threshold voltage shift is considerably less sensitive to the random dopants than to the lateral trap position. We demonstrate that the accuracy of our method is several nanometers. Furthermore, we introduce a compact model which can overcome the time consuming TCAD simulations with little loss in accuracy.

PS.XT14

In this paper, a new method named Incremental Trap-Response (ITR) is proposed for characterizing the time constants of switching oxide traps, which can be used to expand the voltage detectable window of RTN. Both theoretical and experimental results demonstrate that the new ITR method has higher accuracy and is more time-efficient than recently proposed Statistical Trap-Response (STR) method, thus is helpful for trap-related research on both reliability and variability.

PS.XT15

A new embedded-power 120nm technology has been developed offering high performance LDMOS devices for 12V and 24V with a thin 5.2nm gate oxide, a novelty for these voltage classes. We achieved a new industry benchmark of RON equal to 4mΩ×mm2@BVdss=20V. In this paper we show how hot carrier induced dielectric breakdowns (HCIDB) can limit the lifetime of lateral DMOS devices processed with thin oxides.

PS.XT16

The first physics-based model for hot-carrier degradation which is able to capture degradation in both short- and long-channel SiON nMOSFETs is presented. It correctly considers the superposition of multivibrational bond excitation and bond rapture induced by a solitary carrier based on distributed activation energies. The impact of electron-electron scattering on degradation is shown to be crucial in short-channel MOSFETs while the reduction of the activation energy by the oxide field is essential for long-channel devices.

RTN induced variation under the worst bias condition is experimentally investigated for the guard band estimated for design. Moreover, the impacts of BTI aging on RTN are further studied. The experimental results show that RTN amplitude after aging still keeps the same range as that under “time zero” condition. No extra design margin shaving is found considering the interaction between BTI aging and RTN, due to the localized nature of oxide traps.


By studying PBTI on SiON nMOSFETs at the single-defect level we demonstrate a number of similarities between electron capture in nMOS and hole capture in pMOS transistors. Particularly noteworthy are the strong bias dependence of the capture times, switching vs. fixed charge behavior, as well as a strong thermal activation of both capture and emission times. Interestingly, the defect density appears the same, while individual traps have a lower impact on the threshold voltage shift.

Mechanical Stress Effects on p-channel MOSFET Performance and NBTI Reliability, D.P. Ioannou and G. La Rosa, IBM Microelectronics

We report on the impact of mechanical stress on device performance and NBTI reliability of pFETs with identical gate oxide. These effects were investigated by exploiting the well known induced mechanical effects on devices placed in proximity to Through Silicon Vias. The NBTI induced Threshold Voltage shift is found to be unaffected by the mechanical stress, whereas the NBTI component contributing to mobility degradation is strongly dependent on the level of the applied mechanical stress.

THURSDAY MORNING
June 5, 2014

Session 5A - Interconnect Metalization Reliability

Session Co-Chairs: Cathryn J Christiansen, IBM, Howard Gan, SMIC
Kings Ballroom

8:00 a.m.
Session Introduction

8:05 a.m.
5A.1
Electromigration Simulation at Circuit Levels (Invited), C.M. Tan, Nanyang Technological University

Electromigration has been a dominant failure mechanism for interconnects in ULSI. Extensive research works on the understanding of electromigration and methodologies to enhance interconnect EM lifetime are being proposed. While the ultimate goal of all these studies are to extend the interconnect lifetime in ULSI, all the studies so far are on the test structures, with the belief that their effectiveness will be similar
when implemented in circuit level. However, recent studies revealed that this may not be the case, and more considerations are needed when the methodologies are implemented in circuit level. This work shows the need for circuit level electromigration modelling and the method to perform the modelling at circuit level. Examples are shown for digital, analog and RF circuits, and the way to speed up the modelling in complex circuit is also presented, making the method practical for implementation.

8:30 a.m.
5A.2
Electromigration Failure of Circuit – Like Interconnects: Short Length Failure Time Distributions with Active Sinks and Reservoirs, A. Oates and M.H. Lin, TSMC Ltd.

We investigate electromigration failure of Cu/low-k conductors with active (current carrying) sinks and reservoirs. We observe that active sinks lower failure times of via terminated segments, while active reservoirs increase failure times. However, in the latter situation, failures can also occur in the reservoir with lower failure time than via terminated segments. We develop a modeling methodology based on electromigration – induced stress distributions to predict failure distributions in the presence of sinks and reservoirs.

8:55 a.m.
5A.3

A novel model and approach for obtaining improved electromigration short-length effects are reported in this paper. The results for a structure with copper metallization and two width regions demonstrate that increasing the line width for a portion of the line length gives rise to longer electromigration lifetimes. Moreover, the lifetimes are accurately characterized by introducing an equivalent length for the structure that depends on the width and length of each region.

9:20 a.m.
5A.4
Variability Challenges To Electromigration (Em) Lifetime Projections, B. Li, R. Filippi and C. Christiansen, IBM Systems and Technology Group

Controlling the variability could be just as important as improving the median failure times for EM lifetime projections. Understanding the cause of the broad distributions is critical not only for forming process solutions, but also for making the right selection of projection statistics.

9:45 a.m.
5A.5
Scaling Effects on Microstructure and Electromigration Reliability for Cu and Cu(Mn) Interconnects, L. Cao, L. Zhang, P.S. Ho, P. Justison*, and M. Hauschildt*, University of Texas at Austin, *GLOBALFOUNDRIES

EM reliability of Cu(Mn) interconnects was studied by comparing to pure Cu with SiCN and CoWP caps. Microstructure of Cu(Mn) up to 28nm node was investigated using a high-resolution TEM technique. Effects of Mn alloying on EM reliability was examined by extracting interfacial and GB diffusivities together with activation energies from resistance traces for Cu and Cu(Mn) interconnects. Results from microstructure and diffusivities were combined to project Mn alloying effects for future technology nodes.
Session Co-Chairs: Jeff Hicks, Intel, Yung-Huei Lee, TSMC
Kohala Ballroom 1-2
8:00 a.m.
Session Introduction

8:05 a.m.
5B.1

The influence of off-state bias on the time dependent dielectric breakdown of ultra short channel HKMG nMOSFETs is investigated. Under strong DC off-state stress, the dielectric breakdown is caused by hot hole injection. However, under off-state use conditions, CMOS logic justified TDDB with alternating gate and off-state stress appears to have lower life time than the standard DC and AC assessment, which is attributed to continuous charge trapping and detrapping.

8:30 a.m.
5B.2
Time-Dependent Clustering Model versus Combination-Based Approach for BEOL/MOL and FEOL Non-Uniform Dielectric Breakdown: Similarities and Disparities, E. Wu, B. Li, J. Stathis and C. LaRow, IBM Research Division

In this work, we will examine the similarities and disparities between time-dependent clustering model and the combination-based method. We will discuss the constraints of the combination-based approach, particularly in the presence of large number of stochastic random variables in realistic but more complicated cases in comparison with the simplicity of clustering model involving only three parameters. We will demonstrate the general applicability of the clustering model in the case the combination-based approach cannot be applied.

8:55 a.m.
5B.3
Activation of Electrically Silent Defects in the High-k Gate Stack, D. Veksler, G. Bersuker, M.B. Watkin*, and A. Shluger*, SEMATECH, *University College London

We consider the possibility that changes of electrical characteristics of the nFETs high-k gate stacks under low voltage stresses of practical interest are induced primarily by a reversible activation of pre-existing defects rather than generation of new structural defects. Utilizing the multi-phonon-assisted charge transport description it is demonstrated that the trap activation concept allows reproducing a variety of experimental results including stress time dependency of $V_T$, leakage current, CP current, and low frequency noise.

9:20 a.m.
5B.4
Impact of Ionic Drift and Vacancy Defect Passivation on TDDB Statistics and Lifetime Enhancement of Metal Gate High-$\kappa$ Stacks, N. Raghavan, K. Leong Pey, D. Frey* and M. Bosman**, Singapore University of Technology and Design, *Massachusetts Institute of Technology, **A*STAR
Dielectric breakdown, which was perceived to be irreversible, is now well known to be a recoverable process when a reverse-polarity voltage-sweep is applied to the gate stack after soft breakdown (SBD). While the physical role of dielectric and gate electrode on SBD recovery has been addressed in detail recently, this work focuses on applying the percolation model to represent repeated breakdown and recovery events and estimate the enhancement in TDDB lifetime that MG-HK transistors can achieve.

9:45 a.m.
5B.5

A “Detrap-Assisted-Tunneling (DAT)” model is proposed as AC TDDB degradation mechanism for HK/IL stack. For unipolar AC stress, the HK traps are generated during detrap progress, while for bipolar AC stress the holes are injected from substrate to degrade the interfacial layer, thus leads to the AC TDDB lifetime degradation. Fast measurement minimizes the DAT effect, providing a more realistic TDDB lifetime projection.

**Session 5C - MEMS Sensor Reliability**

Session Co-Chairs: Georgios Papaioannou, University of Athens, Michael Nicoladis, IMAG
Kohala Ballroom 4

8:00 a.m.
Session Introduction

8:05 a.m.
5C.1
**Study of Charge Injection and Trapping Mechanisms Responsible for Dielectric Charging in MEMS Switches (Invited)**, F. Souchon

8:30 a.m.
5C.2
**Reliability of High-Q Micromechanical Resonators**, F. Ayazi, Georgia Institute of Technology

High-Q micromechanical resonators are an important class of MEMS devices with growing applications in the areas of timing, sensing, energy harvesting, and wireless communications. Integrated microresonators can have homogeneous or composite structures, and are commonly actuated using capacitive or piezoelectric transducers. They are typically encapsulated using wafer level processes in vacuum to improve their reliability and quality factor and to reduce their overall (packaged) size. Long term stability of the frequency and quality factor of microresonators are influenced by their fabrication processes, encapsulation, and operating conditions. Pure and composite silicon resonators have shown stable operation at high Q factors in excess of 10,000 with reliable hermetic encapsulation. An initial burn-in behavior may exist depending on the structure and fabrication process of the resonator.

8:55 a.m.
5C.3
Dielectric Charging Characterization in MEMS Switches with Insulator-Insulator Contact, D. Molinero, S. Cunningham, D. DeReus and A. Morris, Wispry, Inc.

A dielectric charging characterization is presented based on simple MEMS structures with insulator-insulator contact. Surface charging is generated by triboelectric effects when the MEMS switch is actuated and both insulators are in contact. Hold-down measurements were done to characterize the surface charging in a broad range of voltages and temperature. The results have shown how the key charging parameter is related to the time constant and its variation over temperature.

9:20 a.m.

5C.4

Induced Charging Phenomena on SiN, Dielectric Films Used in RF MEMS Capacitive Switches, M. Koutsoureli, L. Michalas and G. Papaioannou, University of Athens

Contact-less charging process has been found to constitute a compensation mechanism to dielectric charging of MEMS capacitive switches. The present paper aims to provide a better knowledge of induced charging mechanisms that appear in HF PECVD silicon nitride films. The characteristics of this process as well as the degree of compensation has been investigated for different polarization field intensities of both polarities and the results have been correlated to the electrical properties of these films.

9:45 a.m.

5C.5


The influence of temperature distribution caused by dissipated power on Bulk Acoustic Wave (BAW) resonators's behavior has been investigated for the first time. It resulted in an improved modeling of temperature compensated BAW resonators at high power levels by taking the temperature gradient occurring in the layer stack for acoustic and electromagnetic simulations into account. Furthermore it resulted in the avoiding of failures in life time predictions. The results have been verified by appropriate measurements.

Break

10:10 a.m.

Session 5D - Circuit Aging Simulation/Circuits Reliability

Session Co-Chairs: Keith Green, Texas Instruments, Yu Cao, ASU
Kings Ballroom

10:30 a.m.
Session Introduction

10:35 a.m.

5D.1

A new method based on Arbitrary Gate bias Pattern stresses has been successfully developed to measure NBTI in circuit-like condition. It is shown that the arbitrary arrangement of bits during stress does not induce additional degradation compared to standard AC BTI stress. A simple RC model is also shown to be effective to capture the main NBTI features induced by Arbitrary Gate bias Pattern stress.

11:00 a.m.
5D.2

A Numerical Non-Monte-Carlo methodology capable or reproducing circuit output distributions at very high quantiles is presented where arbitrary input distributions can be handled. Flexible simulation setup allows evaluating the workload-dependent BTI impact on circuit performance for usage based scenarios. Application to 6T SRAM in 28nm planar and 14nm and 10nm FinFET technologies.

11:25 a.m.
5D.3

Analog design is facing challenges as reliability requirements are moving into focus as target specifications. Methods providing a degradation-aware design exist, but mostly involve algorithmic optimization. We propose the use of aging-aware sensitivity-maps generated by operating point-dependent degradation within the gm/ID-scheme. Sensitivity-Maps show good alignment with simulated degradation. Different designs of an amplifier structure are investigated by comparing aging-sensitivities and simulated degradation. This technique enables aging-aware design during design phase with comparatively low computational effort.

11:50 a.m.
5D.4
HCI/BTI Coupled Model: The Path For Accurate And Predictive Reliability Simulations, F. Cacho, P. Mora, W. Arfaoui, X. Federspiel and V. Huard, STMicroelectronics

For reliability circuit simulation, native models assumed that their degradations are additive. However, an interaction between these two modes occurs. This paper proposes for the first time to demonstrate that the interaction between BTI and HCI is a “must have” in a DiR model framework. Such a coupled DiR model accurately simulates the degradation obtained on products.

12:15 p.m.
5D.5
An LDMOS Hot Carrier Model for Circuit Reliability Simulation, G. Sasse, J. Claes and B. De Vries, NXP Semiconductors

In this paper we will present a model that can be used to calculate hot carrier degradation in LDMOS devices within a circuit reliability simulation environment. The model is suitable for both nLDMOS and pLDMOS devices. We will show experimental evidence on the applicability of this model over a broad range of VGS and VDS bias as well as temperature.

Session 5E – Memory
Modeling of Crystallization Kinetics in Phase Change Memories for Set and Read Disturb Regimes, N. Ciocchini and D. Ielmini, Politecnico di Milano

This work studies set transition and read disturb in PCM devices. We introduce a new technique for studying crystallization at extremely low currents, which are normally not accessed in set experiments. We develop a model for crystallization in the PCM, accounting for the observed crystallization regimes. Read disturb is studied as a function of the initial state and read current, allowing the development of a unified crystallization model for set and read disturb in PCM.


In this work, we use ab-initio simulations to explore the formation of neutral/charged frenkel-pairs (FP) in CF formation. We propose two possible mechanisms for the FP formation: electron injection and electron detrapping. The two mechanisms are associated with the nature of electrodes. We found that electron detrapping strongly degrades HfO₂ layer. Contrary to non-reactive electrodes with high Wf, we demonstrate that active electrodes with low work function avoid electron detrapping thus improving the device reliability.


In this paper we investigate the high temperature behavior of oxide-based conductive bridge memories. A methodology to optimize both high and low resistance states stability is presented. A numerical model was developed to simulate the filament dissolution over time what allowed us to correlate the filament morphology with the ON and OFF state stability. It is shown that the optimization of the memory operating conditions leads to a stable memory window even at 250°C.


This work studies retention variations in the PCM array (cell-cell statistics) and after repeated set/reset pulses (cycle-cycle statistics). We provide evidence for erratic retention by digital and analog variations
which we attribute to reset-induced changes of the structure and composition in the PCM. A physics model is developed to account for both cell-cell and cycle-cycle retention statistics.

12:15 p.m.

5E.5


We report the first demonstration of in situ biasing and resistive switching of TiO$_2$-based RRAM while observing oxygen vacancy migration under the TEM. Migration of oxygen vacancies forming Wadsley defects was observed as repeated extension and retraction concurrent with SET and RESET processes in single-crystal TiO$_2$ devices. Structural changes within a 20 nm size grain were observed during SET process in ALD-grown TiO$_2$ device using STEM HAADF imaging.

Session 5F - Soft Errors

Session Co-Chairs: Ethan Cannon, Boeing, Norbert Seifert, Intel
Kohala Ballroom 4

10:30 a.m.
Session Introduction

10:35 a.m.

5F.1

IRT (Intel Radiation Tool), a GEANT4 based simulation system for the analysis of radiation-induced single event upsets that accounts for charge sharing effects is described. Charge collection calibration methods, simulation modules and accuracy tradeoffs are discussed. The capabilities and accuracy of the introduced simulation system are demonstrated against measured results for standard and reduced SER devices

11:00 a.m.

5F.2

Experimental results from alpha particle irradiation of 40-nm, 28-nm and 20-nm bulk technology circuits operating in the GHz range suggest that the combinational logic soft error rate (SER) decreases with scaling. However, since the corresponding latch error rate also decreases at a faster rate with scaling, the overall impact of combinational logic soft errors at the chip level is shown to increase. Logic SER predictions for future technology nodes are made.

11:25 a.m.

5F.3
We show the effects of neutron irradiation during accelerated tests on MLC NOR cells down to the 45-nm node, in terms of threshold voltage shifts and error cross section. We discuss the underlying mechanisms and compare the results with published data on NAND Flash. Our accelerated tests and extrapolations suggest field error rates smaller than previously reported from neutron life tests. Retention measurements show that no permanent damage is produced in the upsets cells.

11:50 a.m.
5F.4

A novel pulsed-latch design using hysteresis that operates similar to an edge-triggered flip-flop with improved SER performance is presented. Design was implemented along with standard D-flip-flop and DICE flip-flop in a 20 nm CMOS process. Alpha SER test results indicate ~26× better SER hardness for the pulsed-hysteresis-latch compared to D-FF. The design also benefits from 20% higher speed and has a low area overhead of ~8% over the D-FF.

12:15 p.m.
5F.5

This paper describes the radiation test of a modern 7 stages pipeline microprocessor under heavy ions with an improved software test harness. Crash X-section and failure modes are analyzed and compared with fault injection predictions.

**THURSDAY AFTERNOON**
**June 5, 2014**

**Session 6A – Transistor**

Session Co-Chairs: James H. Stathis, IBM, Souvik Mahapatra, IIT Mumbai
Kings Ballroom

2:25 p.m.
Session Introduction

2:30 PM
6A.1
**Breakdown Mechanisms in MgO Based Magnetic Tunnel Junctions and Correlation with Low Frequency Noise (ESREF)**, S. Amara-Dababi, R.C. Sousa, H. Béa, C. Baraduc, K. Mackay*, B. Dieny, Spintec, University of Grenoble Alpes/CNRS/INAC-CEA, *Crocus Technology

Magnetic tunnel junctions (MTJs) are very attractive for magnetic random access memories (MRAMs), thanks to their combination of non-volatility, speed, low power and endurance. In particular spin transfer torque (STT) RAMs based on STT writing show a very good downsize scalability. However, an issue is that at each write event, the MTJ is submitted to an important electrical stress due to write voltage of the order of half of the electrical breakdown voltage. Here we present a study of breakdown mechanisms in
MgO based MTJ performed under pulsed conditions. We developed a model of charge trapping/detrapping on barrier defects to explain and predict device endurance. We also show that endurance is correlated to low frequency 1/f noise and that such noise measurement could thus be used as a non destructive and predictive tool for the reliability of the devices.

2:55 p.m.

6A.2

Suitability of High-k Gate Oxides for III-V Devices: A PBTI Study in In_{0.53}Ga_{0.47}As Devices with Al_{2}O_{3}, J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns and G. Groeseneken, imec

We present a comprehensive PBTI study in In_{0.53}Ga_{0.47}As devices with Al_{2}O_{3} gate oxide. We found that the stability of the device electrical parameters is limited by a wide distribution of electron traps in the Al_{2}O_{3}, with median energy level close to the channel conduction band. We argue that the superior transport properties of III-V channels will need to be demonstrated with alternative high-k gate stacks in order to be relevant for production.

3:20 p.m.

6A.3


The dependence of NBTI on SiGe thickness and composition for directly grown layers on (100) and (110) Si is studied. SiGe thickness has no significant impact on NBTI at lower Ge%. Lower NBTI was observed with increasing Ge%, even though Npit increases. This improved NBTI is due to bandoffset limited VT, indicating that improvement is substrate related rather than interface related. The physical mechanism is discussed in terms of Ge%-induced variation in band alignment.

3:55 p.m.

6A.4


Deep EOT scaled HKMG p-MOSFETs with different IL (scaled to 1.5Å) are measured by UFM with 10µs delay for both DC and AC stress. A model with ΔVT, ΔVTH [4] and a novel H passivated O vacancy (Ov) related bulk trap generation (ΔVOV) is proposed. The existence of ΔVOV is verified by DFT simulation. The model can predict DC stress and recovery, AC duty (PDC) and f, and gate insulator process impact with consistent set of parameters. Impact of IL scaling on DC and AC NBTI is studied.

4:20 p.m.

6A.5

Bias Temperature Instability Variation on SiON/Poly, HK/MG and Trigate Architectures, C. Prasad, M. Agostinelli, J. Hicks, S. Ramey, C. Auth, K. Mistry, S. Natarajan, P. Packan, I. Post S. Bodapati, M. Giles, S. Gupta, S. Mudanai, and K. Kuhn, Intel Corp.

In this paper, NBTI variation is reported on large data-sets across five generations of Intel technologies (90nm to 22nm) and a comparison of statistical frameworks is utilized to demonstrate the universality of variation metrics across generations. Data-sets of large volumes as well as modeling are reported, and are
emphasized as critical to enable accurate circuit-level assessments through precise simulations of NBTI out to the extreme tail regions.

4:45 p.m.
6A.6
Correlation of BTI Induced Device Parameter Degradation and Variation in Scaled Metal Gate / High-k CMOS Technologies, A. Kerber and T. Nigam, GLOBALFOUNDRIES Inc.

The correlation between time-zero device parameter and BTI induced parameter degradation is studied in detail. A clear correlation for $\Delta I_{\text{dsat}}$ and $\Delta V_{\text{th}}$ to time-zero values is demonstrated. These correlations have a significant impact on the $\sigma$-values of stressed devices and needs to be included in circuit aging simulations.

Session 6B - Circuit Aging Simulation/Circuits Reliability

Session Co-Chairs: Keith Green, Texas Instruments, Yu Cao, ASU
Kohala Ballroom 1-2

2:25 p.m.
Session Introduction

2:30 p.m.
6B.1
Circuit Speed Timing Jitter Increase in Random Logic Operation after NBTI Stress, G. Jiao, J. Lu, J. Campbell, J. Ryan, C. Cheung, C. Young* and G. Bersuker**, NIST, *University of Texas at Dallas, **SEMATECH

Eye-diagram measurement methodology is a useful tool to investigate the impact of stress-induced defects on high-speed (ps) circuit operation and bridges the gap between conventional reliability measurements and “real” circuit degradation. We observe a bit pattern-dependent NBTI-induced increase in timing jitter. Stressed devices measured using a pseudo random binary sequence, which closely approximates random logic, exhibited the largest increase. These observations strongly suggest ring oscillator pattern measurements underestimate circuit impact of NBTI.

2:55 p.m.
6B.2
Fast Characterization of PBTI and NBTI Induced Frequency Shifts under a Realistic Recovery Bias Using a Ring Oscillator Based Circuit, X. Wang, S.-h. Song, A. Paul and C.H. Kim, University of Minnesota

A ring oscillator based circuit for separately characterizing PBTI and NBTI induced frequency shifts is demonstrated in a high-k metal gate process. The proposed design, for the first time, supports AC stress with a realistic recovery condition. Other benefits over the previous works include sub-microsecond measurement time, sub-picosecond resolution and a simple calibration procedure. Detailed stress and recovery measurements under different voltage and temperature test conditions are presented and analyzed.

3:20 p.m.
6B.3
The Impact of Hot Carrier Injection (HCI) on Voltage Control Oscillator Lifetime Prediction, C.-H. Ho, K.A. Jenkins*, H. Ainspan*, E. Ray* and P. Song*, Purdue University, *IBM Thomas J. Watson Research Center

This paper presents a comprehensive study of the impacts of hot carrier injection (HCI) on differential LC voltage controlled oscillator (VCO) reliability tests. It is verified that the stress voltage and operating frequency dependence of time and voltage exponents in the reliability tests are due to the effect of HCI. Based on the observed results, a methodology is proposed to define proper stress conditions for accelerated circuit reliability tests for better lifetime prediction.

3:55 p.m.
6B.4

The fundamental elements of Adaptive Wearout Management is discussed. A new generation of aging monitors which generate pre-error flags to prevent circuit failure with a time window as low as 50ps is demonstrated. AWM voltage regulation is experimentally assessed with 40% static and 25% dynamic power reduction. Finally, we show that the monitoring system is robust with respect to electrical aging. This study offers perspectives of product hardening through adaptive approach to real workloads.

4:20 p.m.
6B.5

As burnin test causes extra test cost, fast and before-burnin device aging prediction is needed. A flow to predict wafers/dies’ speed degradation rate without burnin using ATE test is presented in this paper. The proposed flow is digital with less than 1µs measurement time per die. The accuracy of the proposed flow has been verified by silicon data collected from 5 Freescale wafers from different lots. With the proposed flow, the burnin volume is reduced.

Session 6C - Compound Opto Electronics

Session Co-Chairs: Eric Heller, AFRL, Jose Jimenez, Triquint Semiconductor
Kohala Ballroom 4

2:25 p.m.
Session Introduction

2:30 p.m.
6C.1
Correlating Reliability to Yield for Liftoff Metallization, W. Roesch and D. Hamada, TriQuint Semiconductor

Methods of characterizing and reducing defects is one of the key differences between compound semiconductors and silicon devices. This investigation provides a measure of defectivity for the metallization formation techniques used in compounds that are unique compared to silicon devices. Results show that both physical spacing and voltage are acceleration factors for the failure mechanisms. Relationships between process capability, yield, and reliability will be determined and discussed.
Threshold Voltage Instabilities in D-Mode GaN HEMTs for Power Switching Applications, G. Meneghesso, R. Silvestri, M. Meneghini, A. Cester, E. Zanoni, and G. Verzellesi, University of Padova, University of Modena and Reggio Emilia

Threshold voltage instabilities observed in GaN HEMTs for power switching applications when submitted to either DC or pulsed testing are here presented and interpreted. Two acceptor traps, characterized by two well distinct time constants, are present in the UID GaN channel and C-doped GaN buffer respectively and behave as electron and hole traps respectively. Trap charge/discharge dynamics induces negative and positive threshold voltage instabilities over distinct time scales.

Enhancement of $V_{th}$ Drift for Repetitive Gate Stress Pulses Due to Charge Feedback Effect in GaN MIS-HEMTs, P. Lagger, C. Ostermaier and D. Pogany*, Infineon Technologies Austria AG, *Vienna University of Technology

An enhancement of $V_{th}$ drift in GaN MIS-HEMTs induced by repetitive forward gate bias stress pulses in contrast to single pulses is found. It is revealed that the slope of $\Delta V_{th}$ recovery curves decreases for increasing intermediate-recovery time, i.e. the recovery time in between individual stress pulses. The observations are explained by a charge feedback mechanism. Conclusively, a continuous stress test might underestimate $\Delta V_{th}$ induced by repetitive stress, hence a repetitive stress test is unavoidable.


We show for the first time that there is a distinct fast component to $V_{th}$ drift of GaN MIS-HEMTs under gate stress (PBTI), independent of the gate dielectric material or details of the MISHEMT architecture. Since the trap(s) responsible for this $V_{th}$ degradation component have capture- and emission -times of the order of 10us and 1ms respectively, its impact is not evident in the traditional DC characterization, yet it severely impacts device lifetime projections.

Current Collapse in GaN Heterojunction Field Effect Transistors for High-Voltage Switching Applications, J. Joh, N. Tipirneni, S. Pendharkar and S. Krishnan, Texas Instruments

We investigated the current collapse in GaN HFETs under different high voltage switching conditions. We found that the current collapse under hard switching is lower than that under soft switching due to holes that are generated by impact ionization. The holes compensate the trapped electrons and recover the current collapse. We also showed that surface trapping through gate leakage current is the main cause of soft switching current collapse.

Role of Buffer Doping and Pre-Existing Trap States in the Current Collapse and Degradation of AlGaN/GaN HEMTs, M. Meneghini, I. Rossetto, D. Bisi, A. Stocco, A. Cester, G. Meneghesso, E.
This paper presents an extensive analysis of how buffer doping and reverse bias stress influence current collapse of GaN-based HEMTs: the study is aimed at (i) analyzing the effect of buffer (Fe) doping on current collapse; (ii) at studying the changes in current collapse induced by reverse-bias stress; and (iii) at understanding how traps located into the barrier and into the buffer can contribute to the increase in current collapse detected after stress.